SEMINAIRE

(de **13 h à 14 h**, amphithéâtre, Bât. INP, MINATEC,
ouvert aux chercheurs des autres laboratoires)

Jeudi 14 février 2008

"Techniques de "design" basse consommation au niveau technologique et au niveau circuit : application à la conception d'un System-on-Chip GALS complexe"

par Edit BEIGNE

Abstract: As leakage power and total power is more and more an issue in deep submicron technologies, new design methodologies have to be explored in order to lower the total power consumption in complex System on Chip (SoC) circuits. As the efficiency of power reduction techniques is strongly depending on CMOS devices properties, the correlation between technology and circuit design is first analysed. As technology cannot do all the job at device level, an over-view of design techniques and their power efficiency is presented. This overview leads to a choice of efficient technique to design a complex power aware SoC. A circuit called ALPIN "Asynchro-nous Low Power Innovative Network on Chip (NoC)" has been designed in order to qualify different design techniques at reducing dynamic and static power consumption in a 65 nm CMOS technology. This GALS (Globally Asynchronous Locally Synchronous) circuit is based on a fully asynchronous NoC. Each synchronous island distributed around the NoC is allowed to run from its own local clock generator. Either communication or power modes are handled using a pausable clock technique arranged around each clock domain. Regarding dynamic power consumption reducetion, a global controller is in charge of DVFS (Dynamic Voltage and Frequency Scaling) and IP (circuit units) power On/Off depending on the application. Regarding leakage power reduction, the asynchronous Network-on-Chip is in charge of its own automatic power down during inactivity phases in order to save leakage when no data is flowing through the nodes. Moreover, a PMOS power switch is inserted on each IP blocks and cut in a stand-by mode using an ultra cut-off technique. The physical implementation of this circuit is described using a low power flow at different level of description.

Edith Beigné *received the Electronic Engineering Diploma from the National Polytechnic Institute of Grenoble, France, in 1998. In 1998, she joined the CEA-LETI laboratory in the Center for Innovation in micro & nanotechnology (MINATEC), Grenoble. She was first involved in contacless RFID mixed signal systems. In 2001, she began the asynchronous logic design activity in cryptographic and contacless systems. Around the development of the FAUST project, she has designed a part of the asynchronous Network-On-Chip. Since 2006, she is in charge of ALPIN, a power aware GALS SoC implementing dynamic and static low power techniques based on an asynchronous NoC.*

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