SEMINAIRE

(de 13 h à 14 h, amphithéâtre PHELMA, Bât. INP, MINATEC, ouvert aux chercheurs des autres laboratoires)

Jeudi 14 mars 2013

"mmW circuits in CMOS and perspectives for high-frequency analog circuits using beyond-CMOS technologies"

by José Luis GONZALEZ

Abstract: In the first part of this seminar there will be presented some circuit design alternatives as well as modeling methodologies that have been used in the last years in the development of mmW building blocks and full systems using CMOS technologies. The issues such as process and temperature variations compensation and calibration will be addressed for 60 GHz VCOs and frequency dividers. Some optimization techniques for passives (inductors and varactors) will also be discussed. A whole transceiver system for WirelessHD standard will be used for illustrating the system level impact of mmW blocks design decisions. Following the trend of increase in the operation frequency, this first part will end with a brief overview of CMOS circuit techniques required for close to, or higher than, f_T operation, notably for the 280 GHz band.

In the second part of the seminar the carbon nanotube FET transistor (CNT-FET) will be presented as an alternative for beyond-CMOS integrated circuits. Its very high f_T and other RF figures of merit will be explored, as well as the main sources of variability that are found in the manufacturing process of CNT-FETs. The RF performance of such devices is compared with state of the art CMOS devices and with the predictions of the ITRS roadmap for the forthcoming years. This seminar will conclude with some perspective about the application to high-speed analog circuits of another beyond-CMOS device that has deserved increasing attention during the last years: the Graphene transistor.

José Luis González *(Salamanca, Spain, 1969) received the Diploma in Telecommunications Engineering from Ramon Llull University (URL), Barcelona, Spain, in 1992, an Engineering Degree in Telecommunications Engineering and a PhD (with honors) in Electronic Engineering, from the Universitat Politècnica de Catalunya (UPC), Barcelona, in 1994 and 1998, respectively. He is currently a senior research engineer at CEA-Leti in Grenoble, France. From December 1998 till September 2011 he has been a full-time associate professor at the Department of Electronic Engineering of the UPC's School of Telecommunications Engineering of Barcelona. He was granted a Fulbright Fellowship from January to July 1999 to work as a guest researcher at the University of Arizona, Tucson (USA), where he collaborated with Motorola in the design of high-speed D/A converters. From September 2007 to August 2008 he was a visiting researcher at the STMicroelectronics/CEA-Leti joint Advanced Research Laboratory in Minatec, Grenoble (France), working on the design of mmW oscillators and substrate noise coupling in mmW CMOS ICs. He is the author of 2 books, a book chapter, 17 international journal papers and more than 60 conference papers. He holds 7 patents. His research interests include VLSI design, mixed-signal, RF, mmW and photonics integrated circuits, as well as noise problems in SoC integration.*

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