SEMINAIRE EXCEPTIONNEL

(de 11 h à 12 h, salle Belledonne, IMEP-LaHC, Bât. BCAi, Minatec, ouvert à tous : enseignants, étudiants, chercheurs, administratifs, techniciens)

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"Macroscopic and stochastic aspects of negative bias temperature instability in CMOS devices and circuits"

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Abstract: Negative Bias Temperature Instability (NBTI) is a crucial reliability concern for modern day state-of-the-art CMOS technologies. NBTI results in shift in MOSFET parameters, such as threshold voltage, drain current, etc., over time, and therefore causes long-time failure of CMOS integrated circuits. It is very important to understand the fundamental physical mechanism responsible for NBTI and develop suitable models to predict device and resultant circuit degradation at end product life. In this talk, the underlying physical processes responsible for NBTI in High-K Metal Gate (HKMG) MOSFETs will be briefly reviewed. Defect generation in MOSFET gate oxide will be explained from both macroscopic and stochastic viewpoints, which will be respectively useful to explain NBTI degradation in large and small area devices. This novel simulation framework can explain DC and AC NBTI degradation under various operating conditions such as different operating voltage, temperature, frequency and duty cycle in large area devices, as well as NBTI variability in small area devices. Furthermore, a compact model will be developed to simulate NBTI induced circuit degradation using SPICE simulation, and specific example of variable NBTI impact on SRAM performance parameters, such as read and hold static noise margin and write access time will be discussed.

Souvik Mahapatra *received his PhD in Electrical Engineering from IIT Bombay, Mumbai, India in 1999. During 2000-01, he was with Bell Labs, Lucent Technologies, Murray Hill, NJ, USA. Since 2002 he is with the Department of Electrical Engineering at IIT Bombay and currently holds the position of full professor. His current research interests are in the area of CMOS logic gate stacks - scaling and reliability. He has published more than 150 papers in peer reviewed journals and conferences, delivered invited talks and tutorials in major international conferences including at the IEEE IEDM and IEEE IRPS, and served as a committee member and session chair in several IEEE conferences. He is a fellow of the Indian National Academy of Engineering, senior member of IEEE and a distinguished lecturer of IEEE EDS.*

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