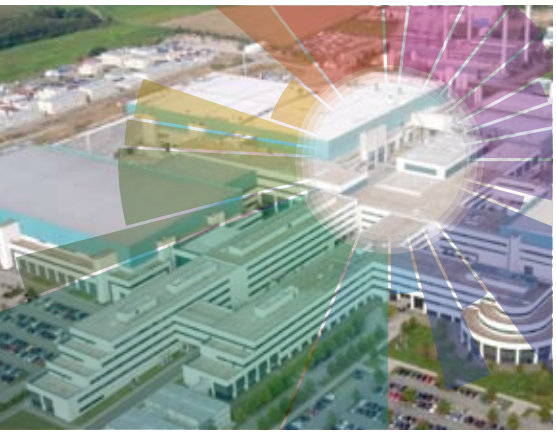
CALL 2012-2

KET Pilot Line Project

PLACES2BE

Pilot Lines for Advanced CMOS Enhanced by SOI in 2x Nodes Built in Europe



To cope with the unacceptably high current leakage and variability, advanced CMOS must introduce novel device architectures in particular for ultra-low power portable applications. The ENIAC JU project PLACES2BE is entirely devoted to the industrialization of 28nm and 20nm Fully Depleted Silicon On Insulator technology platforms, establishing in Europe two different sources supported by the necessary design ecosystem, and exploring the extension to the future 14nm/10nm generations.

Sub Programme

- Semiconductor Process and Integration
- Equipment, Materials and Manufacturing
- Design Technologies
- Communications and Digital Lifestyle
- Energy Efficiency

Objectives

Traditional planar bulk CMOS transistor architecture at present leading edge of miniaturization is plagued by limitations due to unacceptably high current leakages and variability. To cope with these intrinsic limitations there is a need to speed up the deployment and volume manufacturing of innovative CMOS 2X nm technologies with the advantage of Fully Depleted (FD) undoped channel devices. At the moment, there are two main candidate architectures, permitting Fully Depleted undoped channel devices. The first architecture is the 3D FINFET, which uses a gate surrounding the fully depleted channel fin; the second one is the 2D FD Silicon on Insulator (FDSOI) transistor.

The FD Silicon on Insulator (FDSOI) transistor architecture offers a distinct advantage, especially for the Ultra-Low Power applications. FDSOI can be configured to enable a high range Forward and Reverse Body Bias (FBB/RBB), which allows dynamic adjustment of the High Performance / Low Power trade-off of a running circuit or portion of circuit. This unique possibility allows switching from Low Power (LP) to High Performance (HP) modes only when requested and to minimize the overall power consumption which is now the blocking factor for the continuous integration of new functions in battery powered handheld devices.. PLACES2BE is entirely devoted to the FDSOI technology and design deployment in Europe.

The main goal of this project is the industrialization of 28/20nm Fully Depleted (FD) Silicon On Insulator (SOI) technology platforms, enabling 2 different sources in 2 different European countries. The project also plans to establish and reinforce a design ecosystem in Europe using these platforms. Last, it will explore extension towards FD devices at gate length of 14/10nm to continue the evolution toward more efficient technologies.

Work and consortium

PLACES2BE aims at introducing the FDSOI technology for the first time in mainstream digital CMOS for consumer applications, in the Internet multimedia communication field and other applications requiring highly energy efficient digital electronics, such as mixed signal applications addressing wider range of societal needs. PLACES2BE will also exploit the capabilities of the FDSOI advanced CMOS technologies for RF and AMS designs.

This project will achieve the following breakthroughs:

- First 28 nm and then 20 nm FDSOI capacity installed in the World
- First 20 nm CMOS capacity installed in Europe
- Offer of wide dynamic range with the most energy efficient technologies: able to address both low power and high performance applications
- The 28 nm (respectively 20 nm) FDSOI technology should be able to offer 20% performance (speed) improvement over its bulk counterpart at nominal voltage, a wider voltage range operation around 0.4 to 1.2 V with up to a 10x speed boost at 0.4V, as well as a greatly enhanced energy efficiency from 20% in the high operating voltage range to a factor of 2.5 (250%) in the lower operating voltage range.
- Offer the capability to dynamically adjust the devices performance / power trade-off thanks to the back biasing feature.

For achieving success the project will implement a number of activities in parallel and will be carried by a large project consortium expanded to include all necessary competencies and contributions:

- Technology Robustness
- Multiple source enablement
- Technology Design enablement
- State of the art demonstrators and prototypes
- Reliability of technology and of design
- Forward looking studies to prepare the next technology nodes (14/10nm)

Impact

The expected impact of the proposed innovation deployed in PLACES2BE will be

- Strengthening the nanoelectronics manufacturing capabilities in Europe.
- Reinforcing the European IP and Fabless ecosystem.
- Solidifying the relationship between industry and academia throughout Europe.

PLACES2BE Pilot line aims at implementing 2 physical PLACES where those innovations can be industrialized, benefiting the whole value chain: from device physics, to equipment assessment, technology development, modelling, CAD tools, design, and applications. PLACES2BE is therefore also a distributed research infrastructure in the nanoCMOS domain. Beyond the direct impact induced by the material and intellectual investment, it will positively impact the whole value chain of digital electronics in Europe.

Semiconductor Process and Integration

Partners

- STMicroelectonics (Crolles 2) SAS
- STMicroelectronics SA
- STMicroelectonics SAS Grenoble
- ST-Ericsson (Grenoble) SAS
- Commissariat à l'énergie atomique et aux énergies alternatives (CEA/LETI)
- SOITEC SA
- Adixen Vacuum Products
- Mentor Graphics France Sarl
- Ion Beam Services
- Institut Polytechnique de Grenoble
- Dolphin
- Université Catholique de Louvain
- Interuniversitair Micro-Electronica Centrum vzw (IMEC)
- ST-Ericsson Oy (Finland)
- GlobalFoundries
- Forschungzentrum Jülich GmbH
- University of Twente
- Axiom
- Bruco Integrated Circuits
- eSilicon
- ACREO
- ST-Ericsson AB
- Ericsson AB

Project co-ordinator:

- François Finck, STMicroelectronics

Key project dates:

- Start: 03.12.2012
- Finish: 31.12.2015

Countries involved:

- Belgium
- Finland
- France
- Germany
- Romania
- Sweden
- The Netherlands

Total budget:

- € 358.8 million

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