INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

European and International Nanolectronic Roadmaps: from Materials to Systems

IMEP-LAHC, April 29, 2020

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IMEP-LAHC

HORIZON 2020

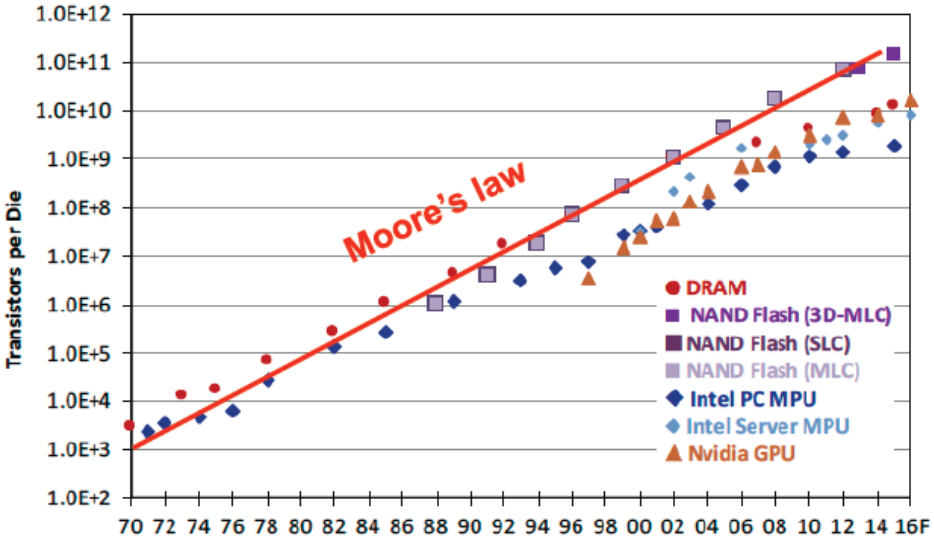
ICT-CSA: Micro- and Nano-Electronics Technologies
Grant Agreement n° 685559

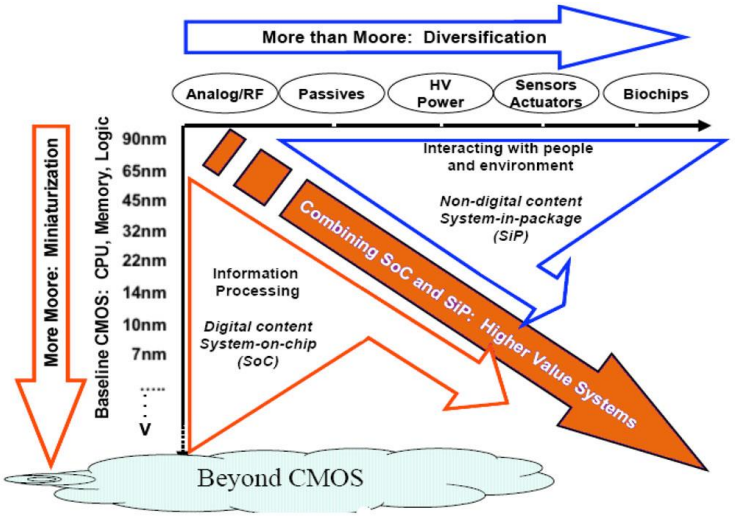
Change of paradigm for many applications

From More Moore …

… to …

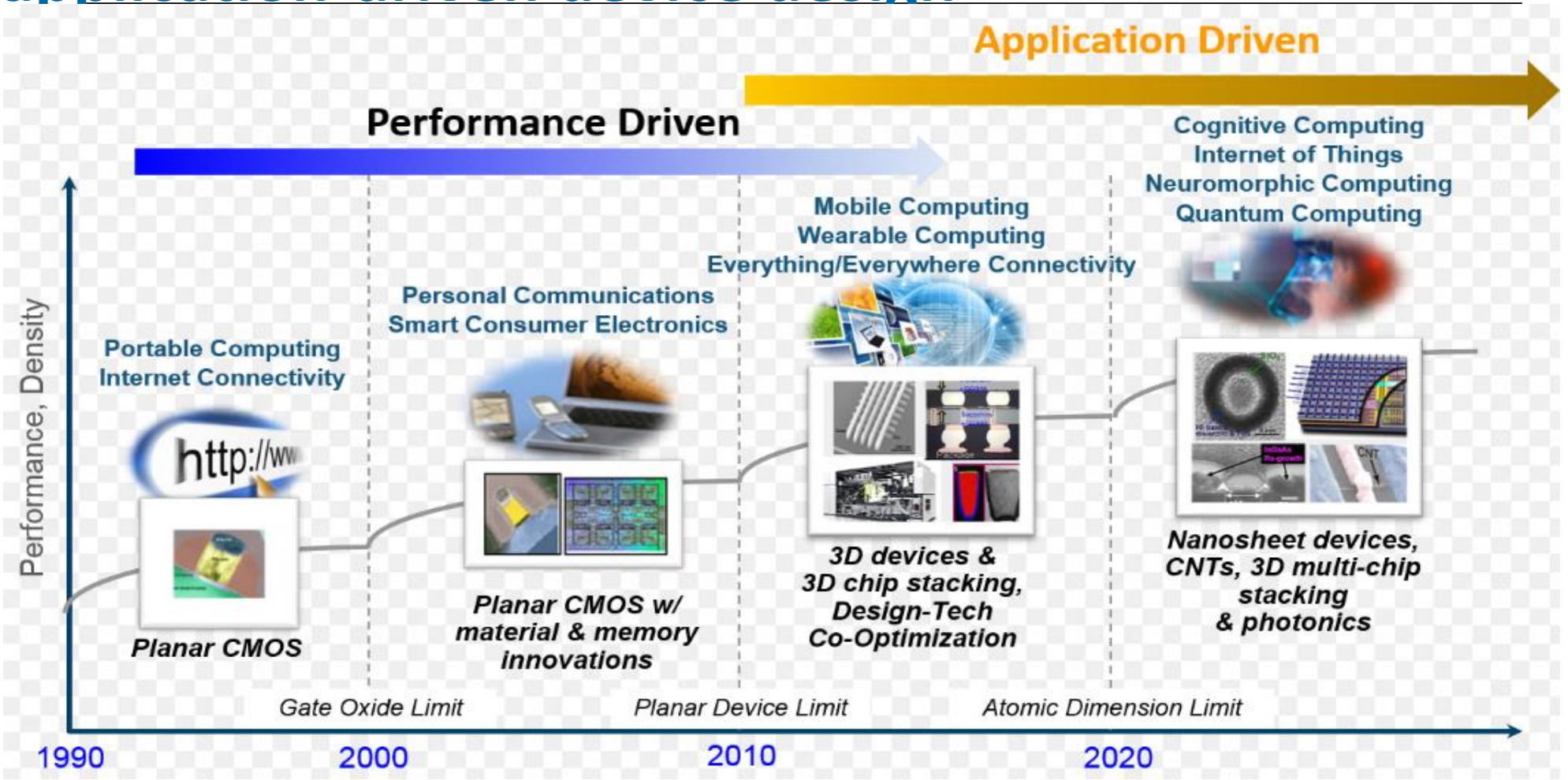
More than Moore and heterogeneous integration





- From device density … … to … … functionality increase
- From device cost driven … … to … … system cost driven
- From single figure of merit … … to … … multiple parameters
- From Technology push … … to … … Application pull
  … full supply chain
  … sustainability

At the same time: **From performance-driven to application-driven device design**



Source: IBM

Complementarities: NEREID –ECS SRA - IRDS






From Applications …

different

different

E C S

NEREID

IRDS

International Roadmap for Devices and Systems

Roadmap

Different Timescale, Topics, Method, Figures of Merit

Different focus: Computing vs non Computing



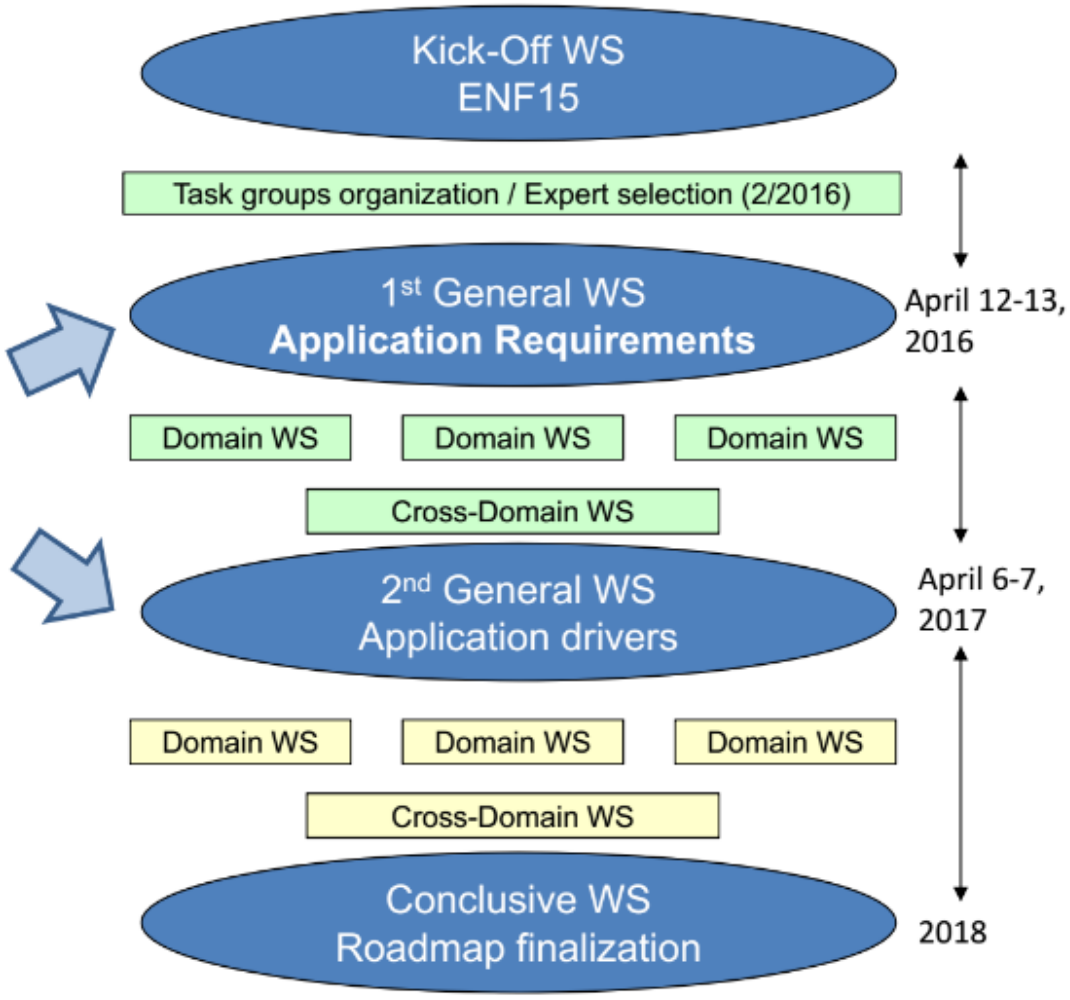
… to European strategic programs

NEREID Roadmap Process

- From European application needs to specific technical workshops

  - Automotive
  - Medical
  - Security
  - Energy
  - Industrial
  - IoT
  - Mobile convergence

- Large participation of (>100 !) experts (internal, external ; application, technology) from leading European academic and industrial institutions in Workshops



NEREID Structure & coordination with other regions

Management

Communication & Dissemination

Beyond CMOS

Advanced Logic and Connectivity

Functional diversification

System Design & Heterogeneous Integration

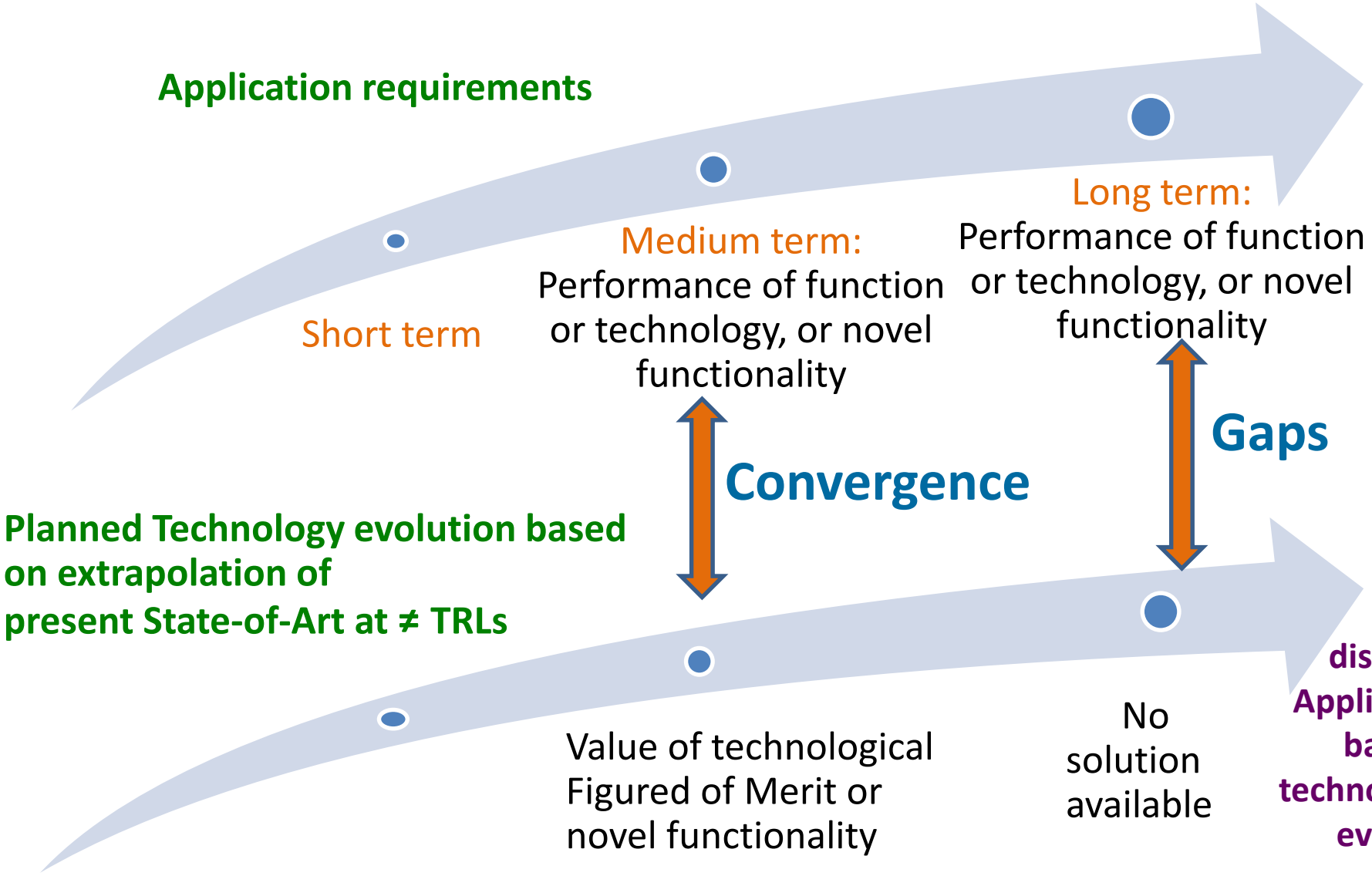
Equipment & Manufacturing Science

Coordination with roadmap initiatives

Advisory Committee

10-15 high level members:
Europe, USA, Asia

The NEREID Approach



IRDS Chapters

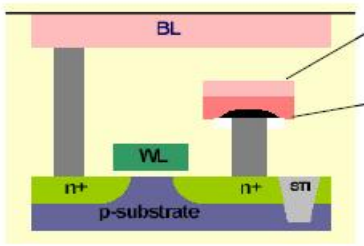
- Application Benchmarking
- System and Architecture
- More Moore
- Beyond CMOS and Emerging Research Materials
- Cryogenic Electronics & Quantum Information Processing
- Outside System Connectivity
- Yield Enhancement
- Factory Integration
- Lithography
- Environment, Health, Safety and Sustainability
- Metrology
- Packaging Integration

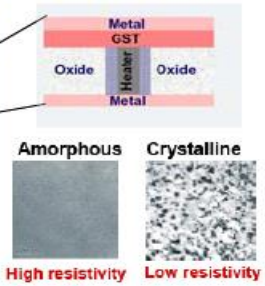
Advanced Logic / *Nanoscale FETs*
(NEREID & IRDS)

Nanoscale device roadmap for low energy, scaling, high perf., new functionalities

… IC evolution …

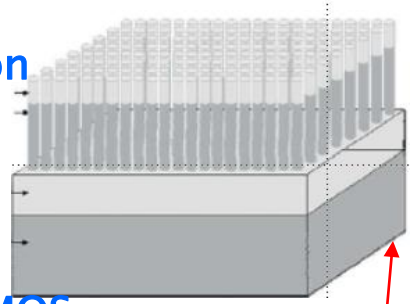
NEMS



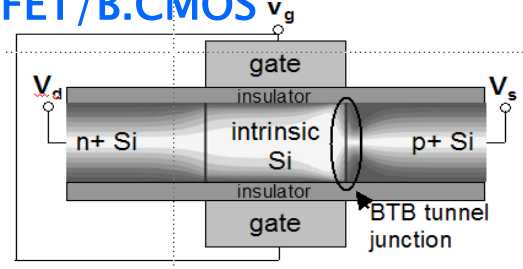


Non-charge/
PCRAM

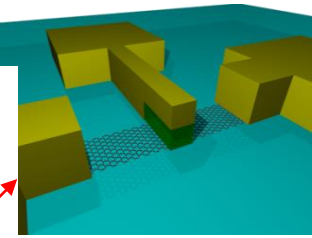
NW/Carbon
-based
MtM



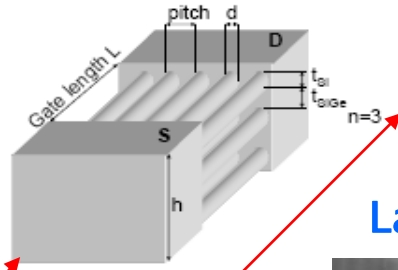
TFET/B.CMOS



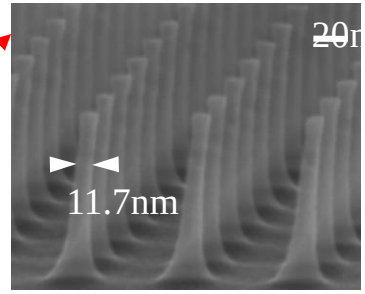
Nanosheet/2D-FET



3D-NW

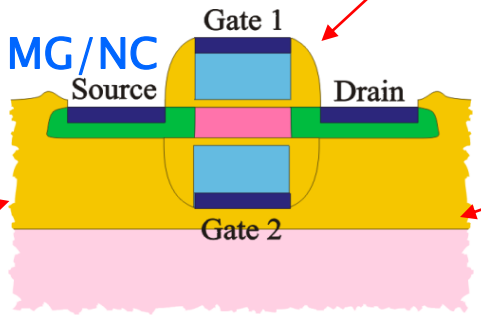


Lateral/Vertical

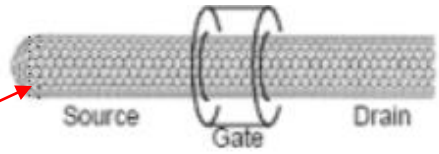


NWFET/NVM

MG/NC

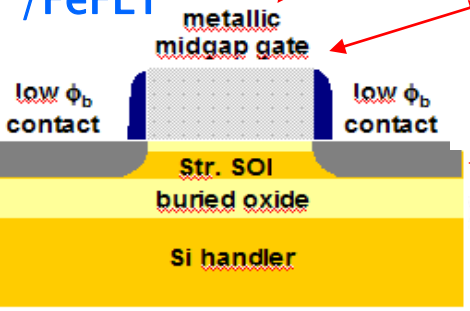


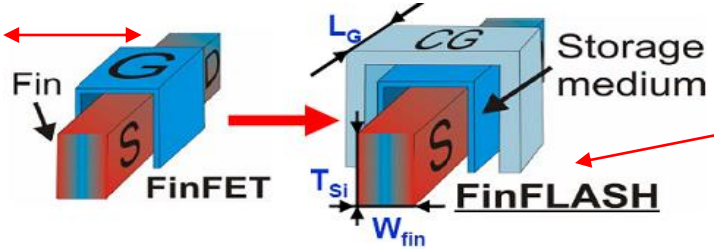
MC

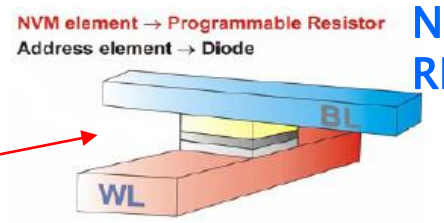


CNTFET

FDSOI/NCFET
/FeFET







Non-charge/
RRAM/MRAM

… IC evolution …

Challenges for future Nanoscale devices

-High performance

-Low/very low static and dynamic power consumption

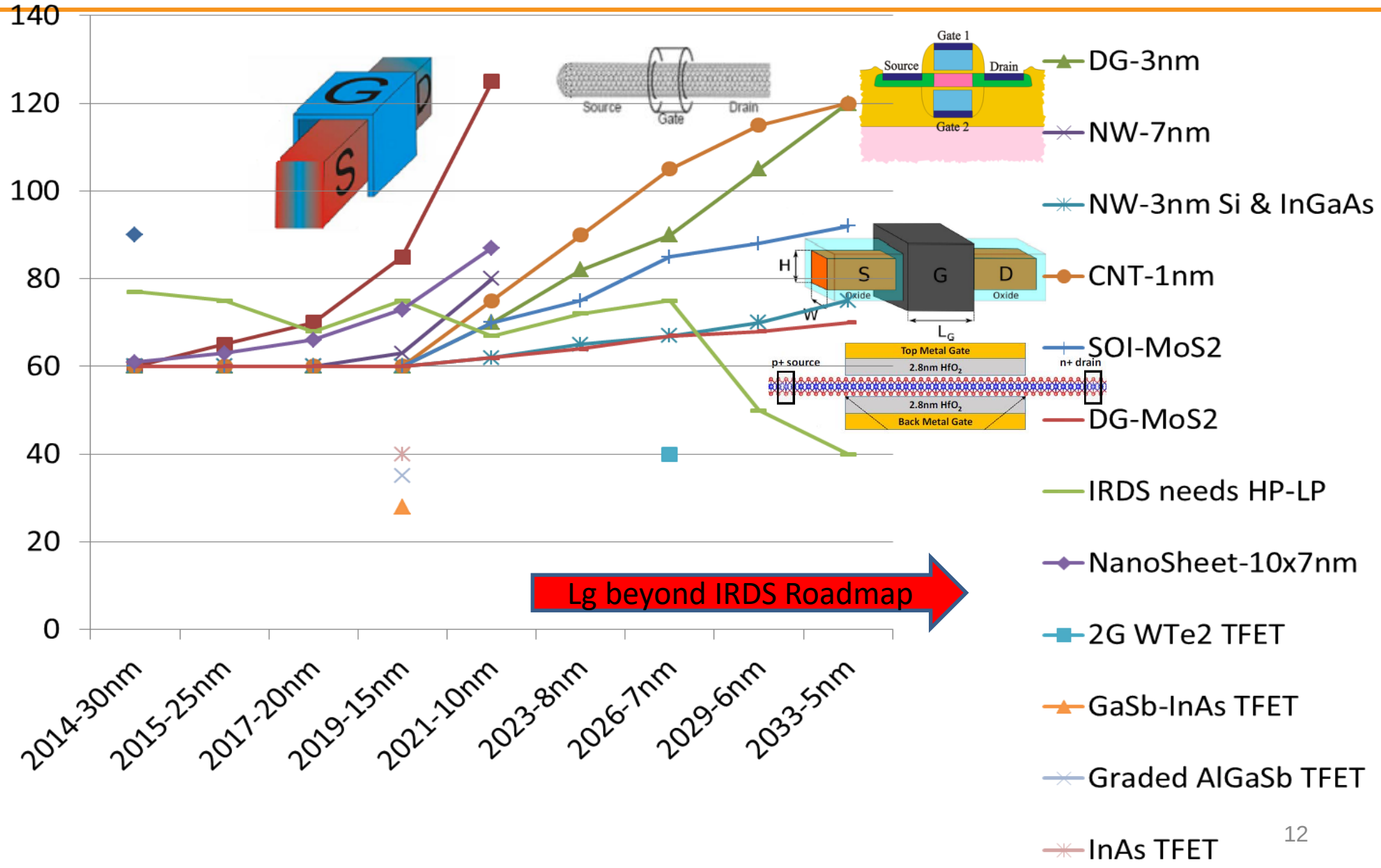
-Scaling

-Low variability

-Good reliability

-Affordable cost

Sub. Swing vs Year / Lg (mV/dec)*(Sim.)*

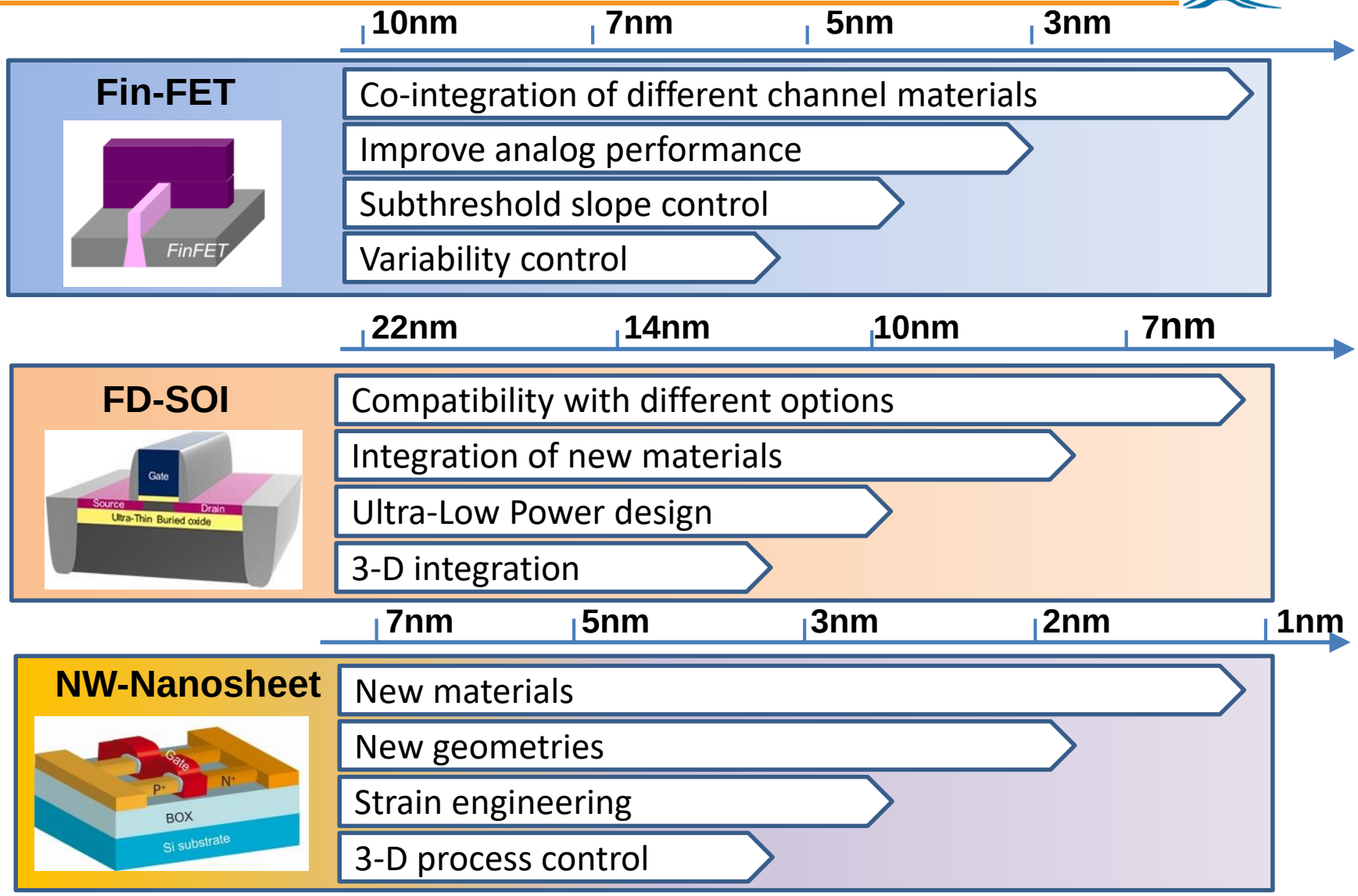


Research Priorities

Advanced Logic and Memories
(NEREID TASK 3.1)

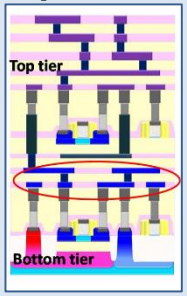
- Nanowires
- FinFET
- FD-SOI
- Negative Capacitance FET (NCFET)
- Carbon Nanotubes (CNTFET)
- Memories, Concept 1 - OxRAM:
- Memories, Concept 2 - CBRAM
- Memories, Concept 3 - PCM
- Memories, Concept 4 - MRAM
- 3D sequential integration
- Reliability, Characterization, Modelling

Nanoscale FETs: Research highways



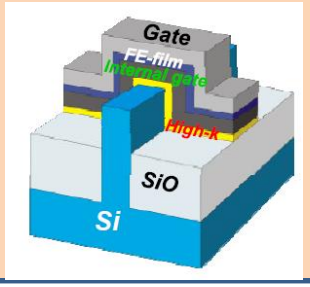
Nanoscale FETs: Research highways

Sequential 3D



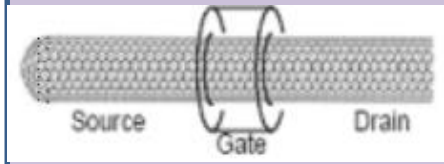
- Ultra-fine grain interconnections between layers
- Thermal management/self-heating mitigation
- Design Tools for place and route
- Manufacturing challenges

NCFET



- Identify the maximum switching speed
- Investigate the scaling potential of the device
- Investigate the impact of hysteresis at design level
- Develop thin Hafnium based Ferroelectric layers with low coercive field

CNTFET

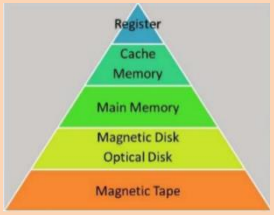


- Develop solutions to remove the metallic CNTs
- Develop faster growing process
- Develop solutions to lower the Schottky barriers at source/drain
- Develop circuit design strategies to deal with variability

Nanoscale FETs: Research highways

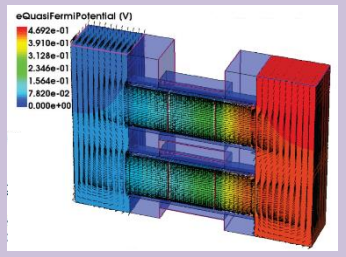
Non Charge-based memories

OxRAM
CBRAM
FeRAM
MRAM
PCRAM



- Threshold spread and variability control
- Reliability and thermal stability
- Cell architectures for scalability
- New materials

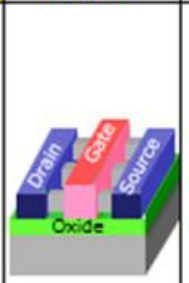
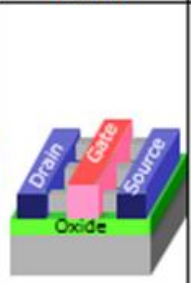
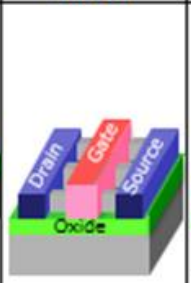
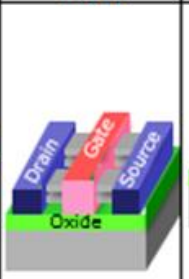
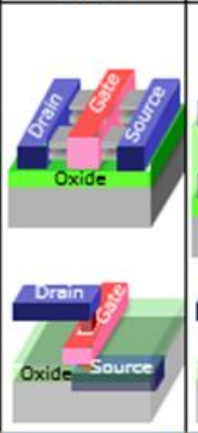
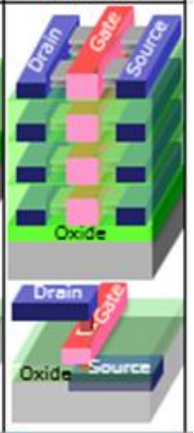
Charact. & Modelling



- Modelling and charact. of new materials, including confined ones (2D, 1D)
- Modelling and charact. of technology and process including 3D
- Modelling and charact. of variability and reliability
- Models and charact. of novel device concepts

IRDS Roadmap 2018

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

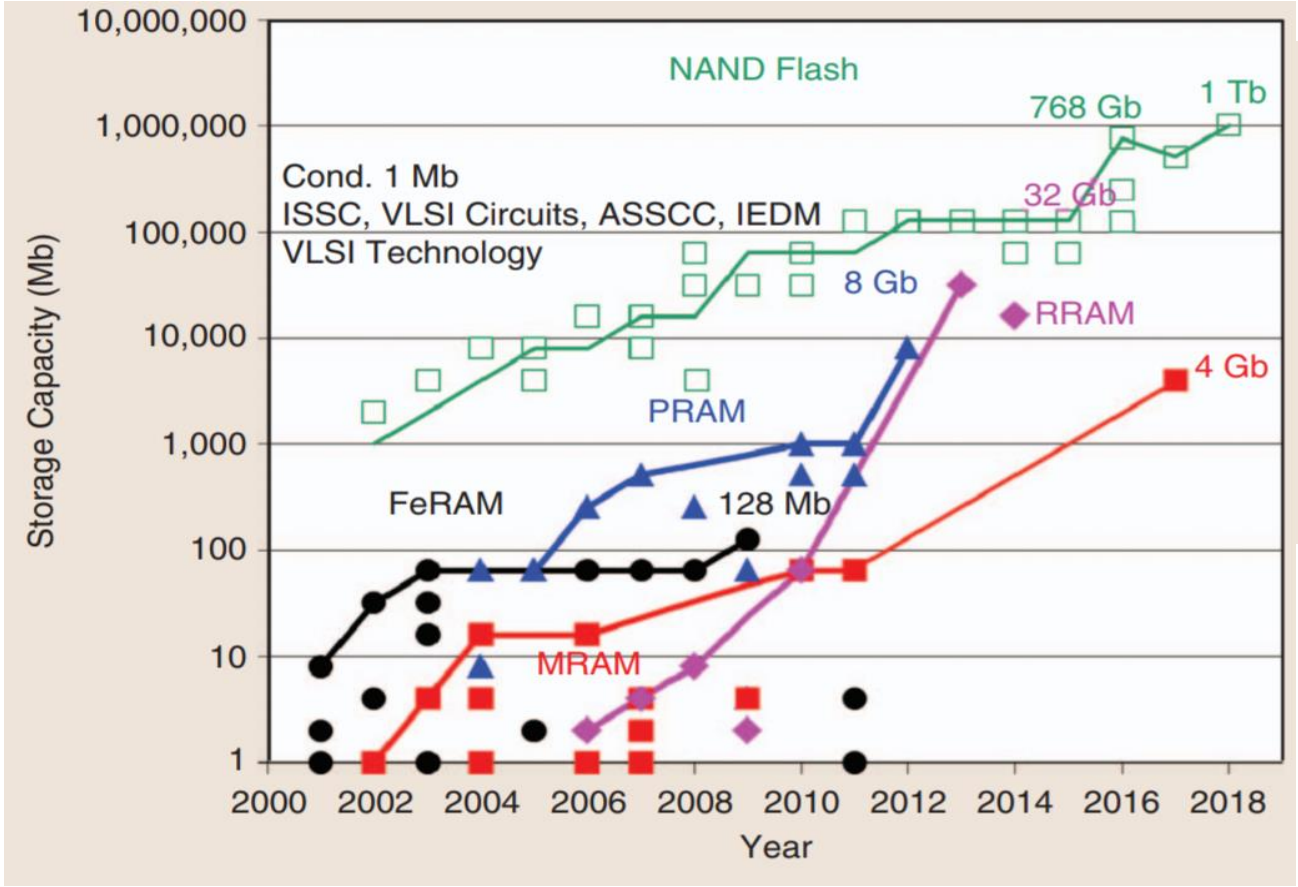
YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
							
LOGIC DEVICE GROUND RULES							
Mx pitch (nm)	40	36	32	24	20	16	16
M1 pitch (nm)	36	32	30	21	20	20	20
M0 pitch (nm)	36	30	24	21	16	16	16
Gate pitch (nm)	54	48	45	42	40	40	40
L_g: Gate Length - HP (nm)	20	18	16	14	12	12	12
Beyond-CMOS as complimentary to mainstream CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	Si	SiGe25%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat

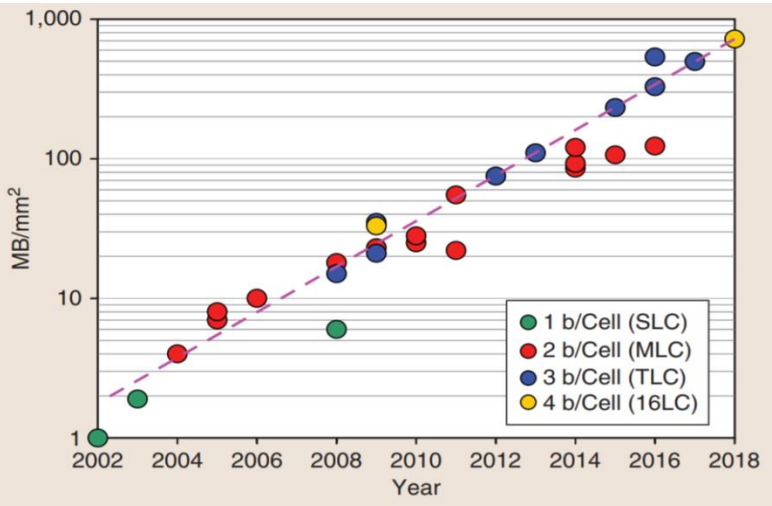
3D NAND – IRDS roadmap

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
FLASH TECHNOLOGY							
2D NAND Flash uncontacted poly 1/2 pitch – F (nm) [1][2]	15	15	15	15	15	15	15
3D NAND minimum array 1/2 pitch - F(nm) [3]	80	80	80	<80	<80	<80	<80
Number of word lines in one 3D NAND string [4]	48-64	64-96	96-128	128-192	256-384?	384-512?	512+?
Dominant Cell type (FG, CT, 3D, etc.) [5]	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D
Product highest density (2D or 3D)	512G	1T	1T	1.5T	3T	4T	4T+
3D NAND number of memory layers [6]	48-64	64-96	96-128	128-192	256-384?	384-512?	512+?
Maximum number of bits per cell for 2D NAND [7]	3	3	3	3	3	3	3
Maximum number of bits per cell for 3D NAND [8]	3	4	4	4	4	4	4
Chip area at maximum number of bits (mm^2) [9]	140	140	140	140	140	140	140
Bit density at maximum number of bits/cell (Bits/cm2) [10]	3.66E+11	7.31E+11	9.75E+11	1.46E+12	2.93E+12	3.90E+12	?

- 2018: 64-96 layers, 0.7-1 Tbits
- 2034: 512+ layers, >6 Tbits

1Tb (64 layers, 4b/cell) 3D-NAND





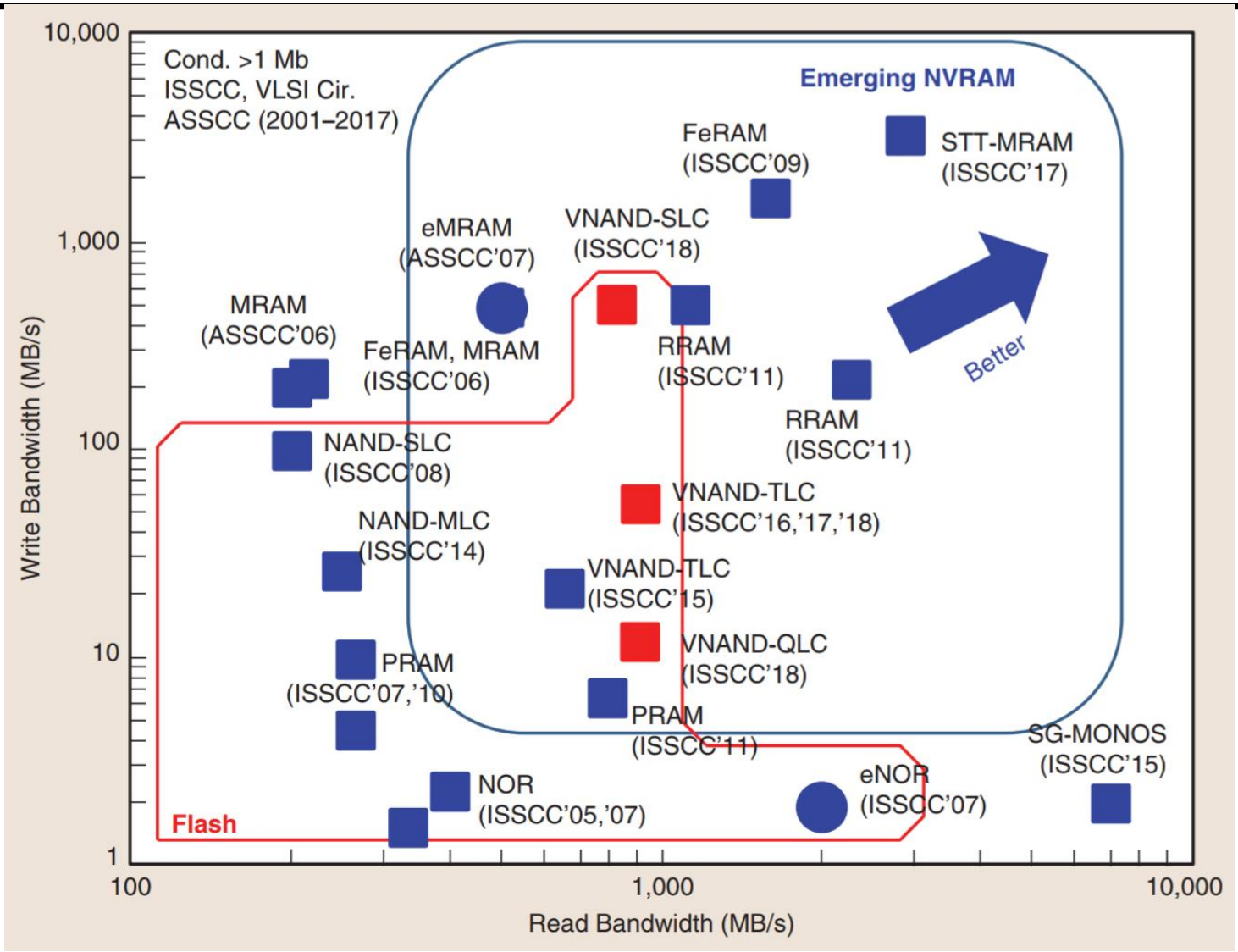
1-Tb NAND Flash memory in 64 stacked layers using 4-b/cell technology with 5.63-Gb/mm2 areal density

512-Gb 3-b/cell 3-D Flash memory on a 96-word-line-layer technology

Source: ISSCC 2018

IEEE

Non-charge-based memories for embedded applic.



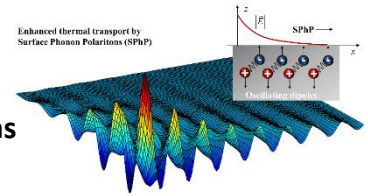
IEEE

Beyond-CMOS
(NEREID & IRDS)

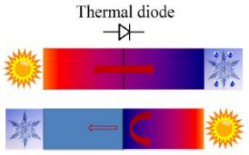
Opportunities in the Beyond CMOS field

- New **state/hybrid state variables**: spin, magnon, phonon, photon, electron-phonon, photon-superconducting qubit, photon-magnon, etc…
- States can be digital, multilevel, analog, entangled…
- **Low power**: Spintronics, magnons, even entropy-based computing
- **High speed**: 2D systems, valleytronics (~100 fs relaxation times)
- Applications in information processing: **best suitable variables can be combined for efficient operation** (e.g. optomechanics for light to mm-wave conversion, neuromorphics for various pattern recognition tasks)

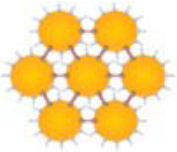
Surface phonon polaritons



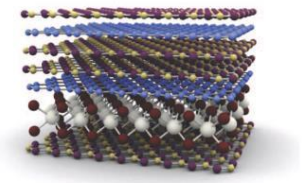
Thermal computing

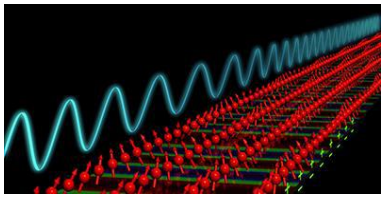


Molecular electronics



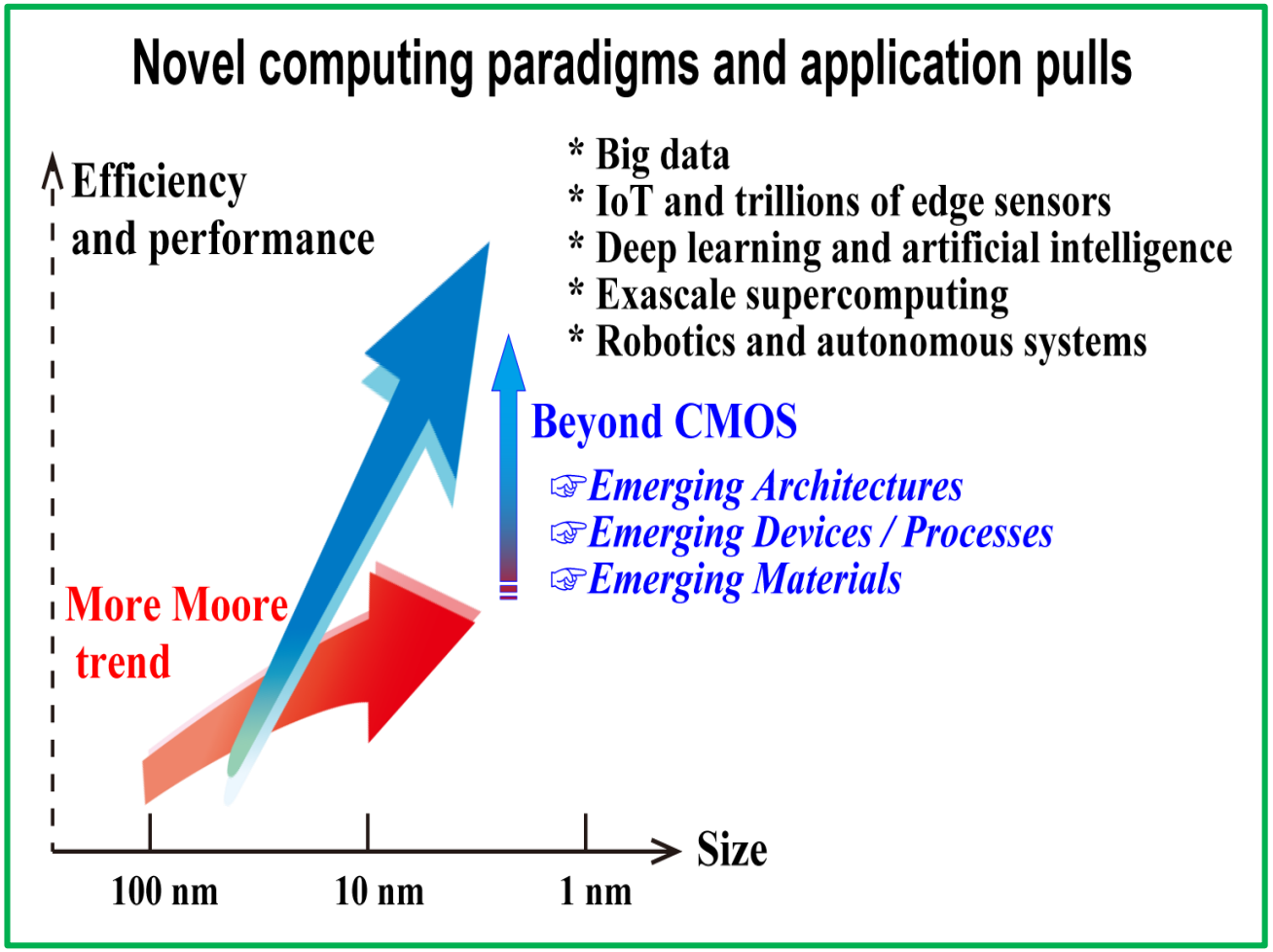
2D materials



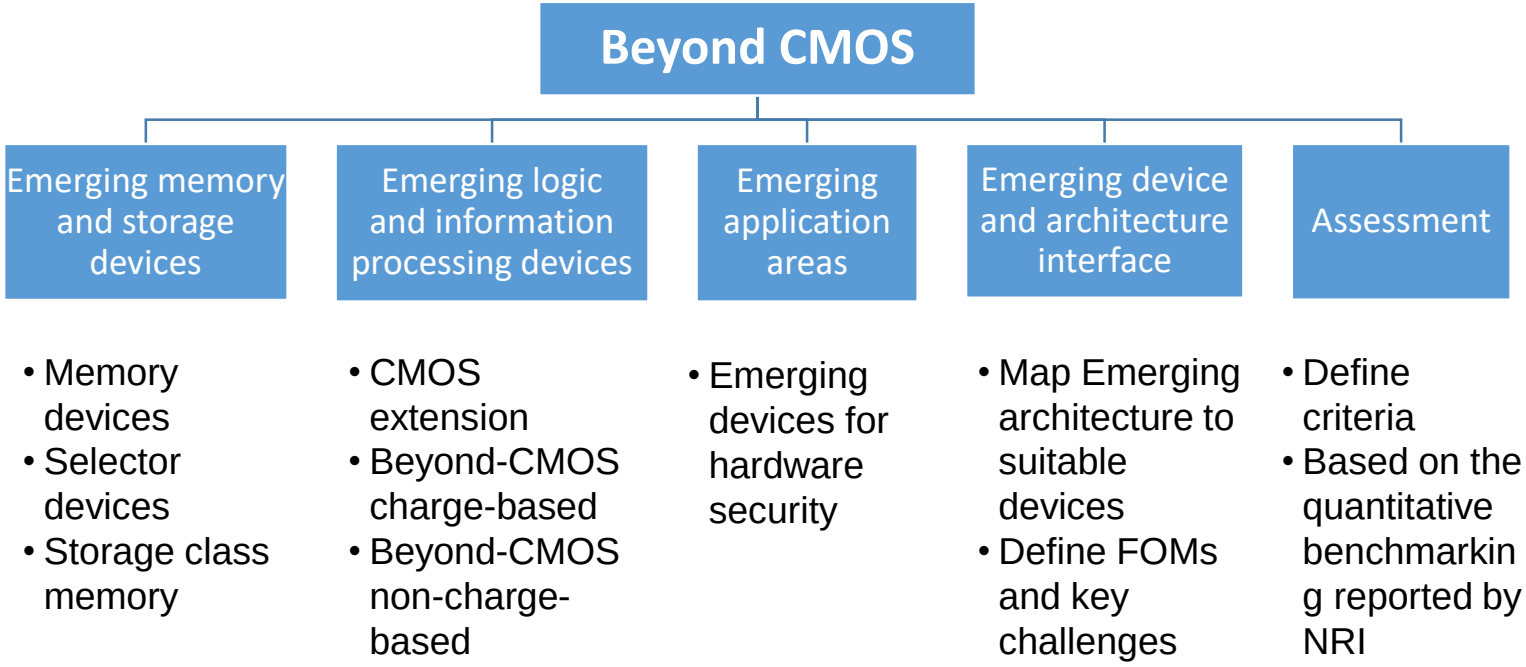


Magnons

Objective of Beyond CMOS Chapter

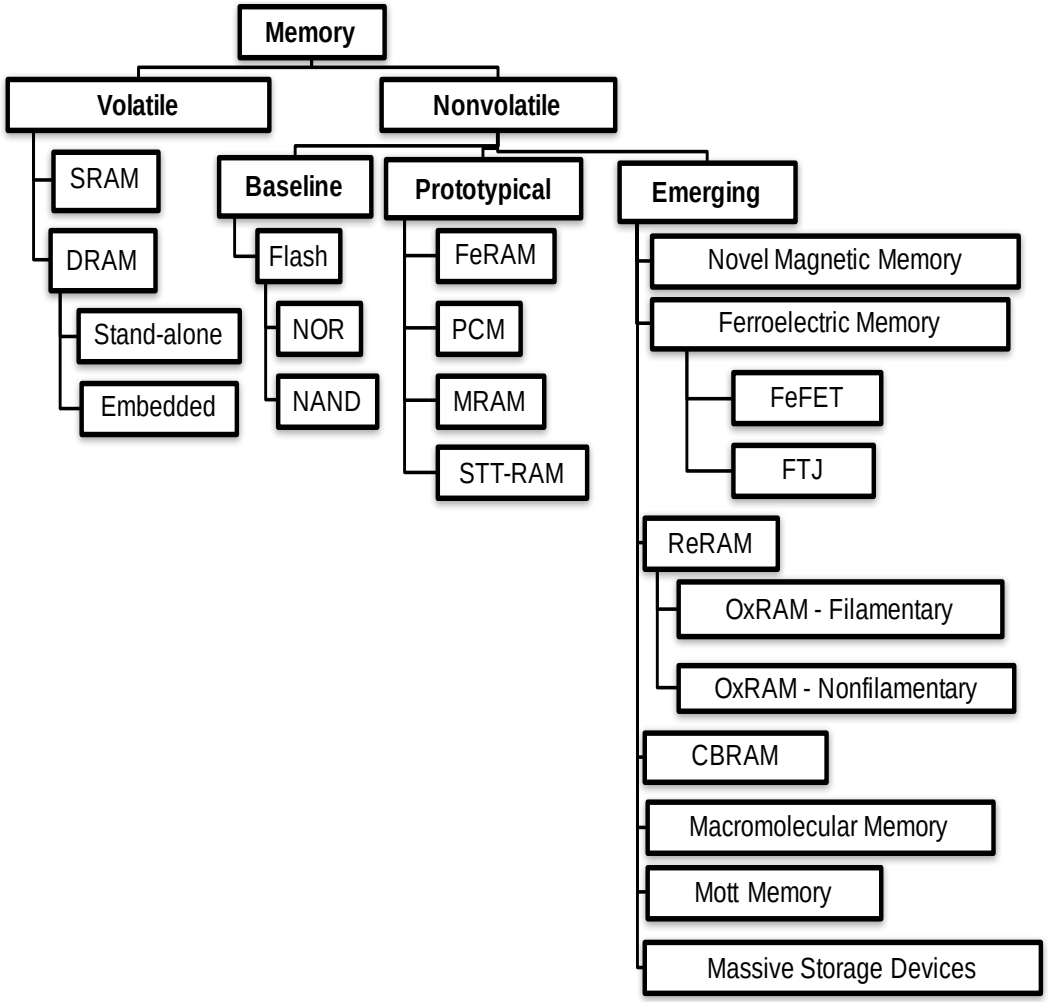


BC Chapter Organization

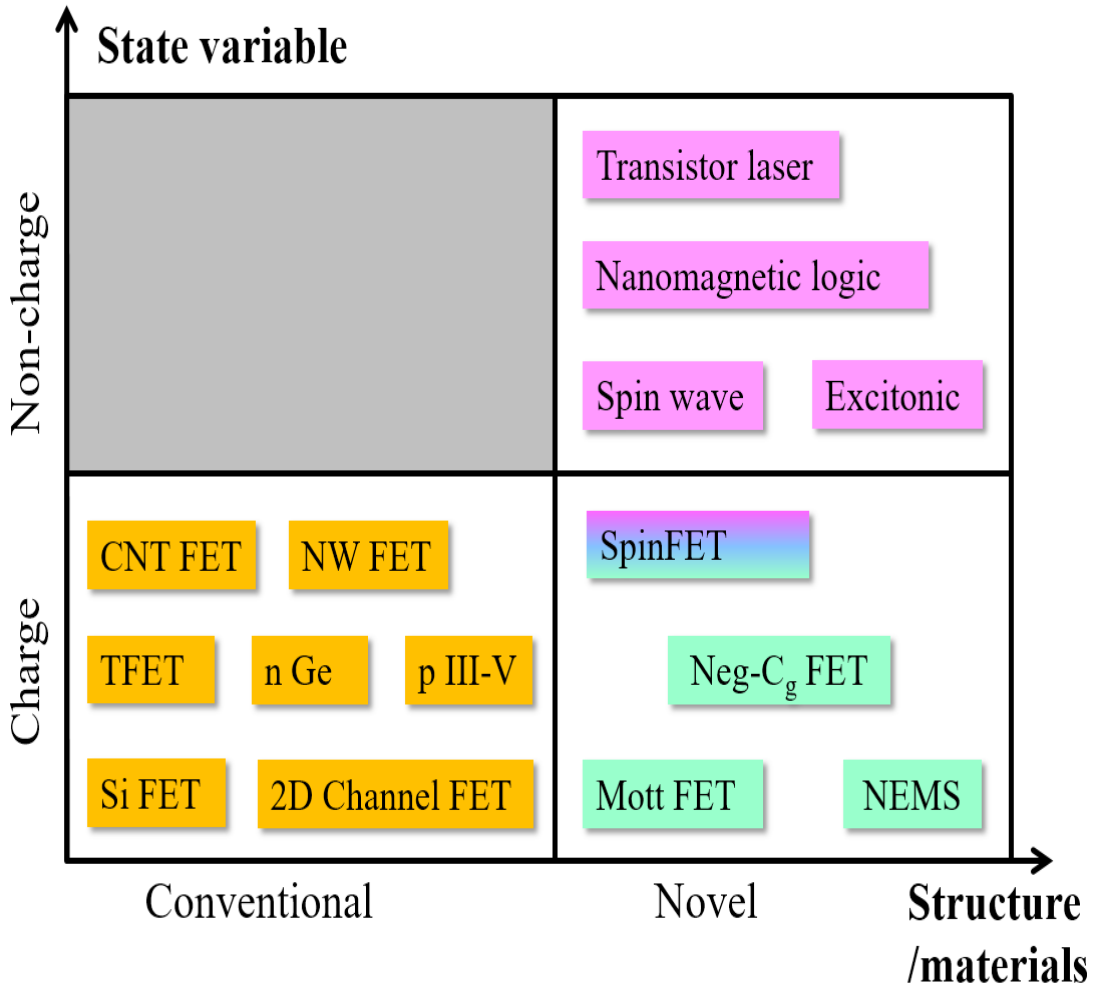


"Emerging Research Materials" will be rolled into the Beyond-CMOS chapter

Emerging Memory Devices



Logic and Information Processing Devices



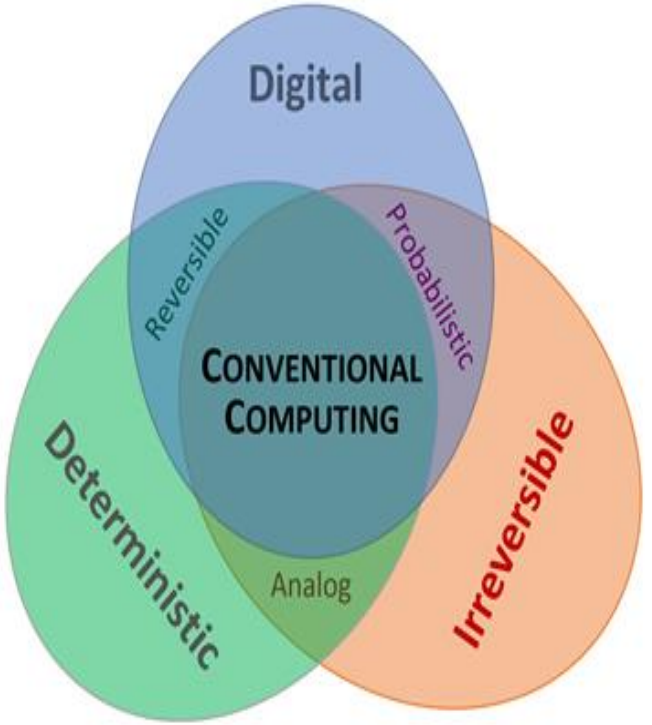
IRDS Emerging Research Materials for:

- More Moore
- Logic (Structure (finFET, LGAA, VGAA), channel material (Si, SiGe, Ge, III-V), Doping, Contacts, Gate Stack)
- Memory (DRAM, NVM)
- Beyond CMOS
- Emerging logic and information processing (2D materials, CNTs, spin, Mott, negative capacitance, nanomagnetic, excitonic, photonic, NEMS)
- Emerging memory and select (ReRAM, magnetic, ferroelectric, Mott)
- Lithography and patterning
- Interconnect
- Packaging and heterogeneous integration
- Outside system connectivity
- Emerging and/or disruptive convergent technologies (Mobile, IoT, Sensors, Energy, Medical)

Emerging Device-Architecture Interaction

- Analog computation
  - Analog crossbar architectures
    - Matrix vector multiplication (MVM) and vector matrix multiplication (VMM)
    - Outer product update (OPU)
    - Field programmable analog array (FPAA)
    - Resistive memory crossbar solver
    - Ternary content addressable memory
  - Neural computing and crossbar architectures
    - Analog neuron functional block (ANFB)
    - Magnetic cellular neural network
  - Computing with dynamical systems
    - Computing with coupled oscillators
    - Chaotic logic
  - Analog architecture and energy minimization

- Probabilistic circuits
- Reversible computing



Categorization of conventional vs. alternative computing paradigms

Research Priorities

Criteria:

- **Potential for data processing**
- **Time scale ~10-15 years**

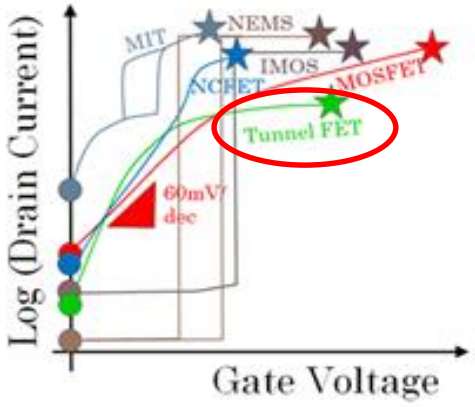
Beyond-CMOS – Emerging devices and Computing Paradigms (NEREID Workpackage 2, WP2)

- Steep slope switches: Tunnel FETs
- Neuromorphic circuits and computing
- Spintronics
- Quantum Photonics
- Phonon, Brownian and nano-opto-mechanical computing

Tunnel FETs

Opportunities

Small slope switches



- Operation based on band-to-band tunneling
- Sub-thermionic subthreshold slope, S<60 mV/dec at RT
- Supply voltage scaling -> 0.2-0.3 V
- Low power consumption
- Von Neumann architecture applies -> compatible with current circuit designs
- 2D/2D TFET architecture
- Analog gain at low I/V

Challenges

- Low I_{ON} -> Low operation speed
- Materials and interfaces (traps degrade the operation)
- Scaling may be an issue
- Design tools for TFET circuitry are missing

Neuromorphic Computing

Opportunities

- Two approaches:
  - HPC + algorithms, pattern recognition, data mining
  - Specific hardware (digital, analog, mixed) with memory nodes
- Integration with CMOS platform
- Low power, high efficiency (sub-fJ energy per bit possible)
- Supervised/unsupervised learning
- Fast pattern recognition (images, text, medical etc.)
- Photonic synapses (optical fibres + PCM synapses)
- Degrees of freedom: Weighting of input can be multilevel, parallel or serial

Challenges

–Hardware development (CMOS neurons and PCM synapses, ...)

–Material issues, CMOS compatibility

–Non-von Neumann architectures, algorithms…

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Spintronics

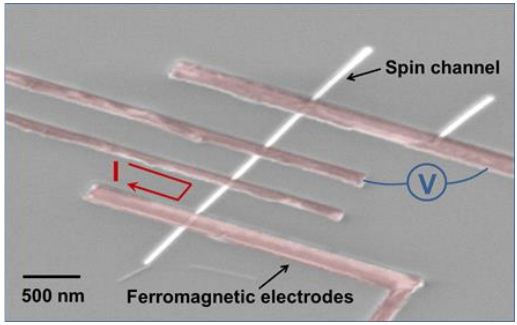
Opportunities

- Established technology for memories, STT-MRAM market growing
- Spins can be extra degrees of freedom in information processing
- Spin waves/magnons: No Joule heating, potential for THz operation
- Logic circuits have been demonstrated (switches, XNOR, majority gates)
- Fewer components, smaller footprint, low power consumption
- Neural networks have been demonstrated
- Tens of GHz microwave oscillators based on spin torque and spin Hall effect
- Topological insulators have potential for robust interconnects

Challenges

- Materials, interface and processing issues challenging
- Spin injection and read-out in spin FETs
- Magnetic field required in some cases

SEM image of a spin-valve device in which the charge and spin currents are separated



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Beyond-CMOS: Research Highways

- Nanofabrication affects most of the emerging technologies impacting variability of critical dimensions and processing defects. Novel approaches are required for *dimensional and compositional nanometrology*, accompanied by a traceable measurement protocol and to-be-developed instrumentation
- Manufacturability (non-standard processes, bottom-up approach in many cases, tolerances, lab-scale)
- Operation conditions (temperature, magnetic field…)
- Architectures (interconnects, variability, amplification, various functions for logic operations, memory, programming)
- Figure of Merits difficult to define before standardization (different operation principles for each area/technology)
- Identify common technological and design challenges to most emerging Beyond CMOS approaches as first step to overcome them and advance to higher TRLs.
- Foster collaborative projects between Academia and Industry on long term topics

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Cryogenic Electronics and Quantum Information Processing (IRDS)

-Superconductor Electronics

-Cryogenic Semiconductor Electronics

-Quantum Information Processing

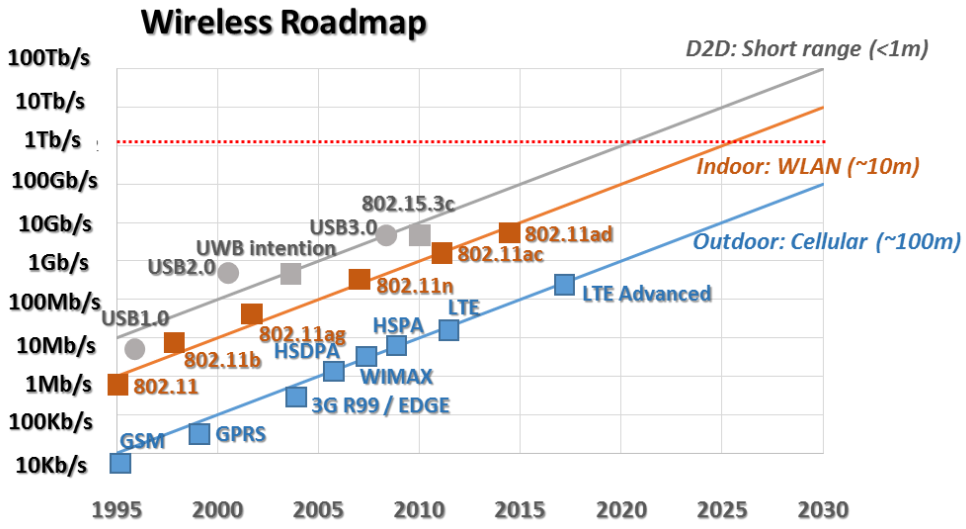
Connectivity
(NEREID & IRDS)

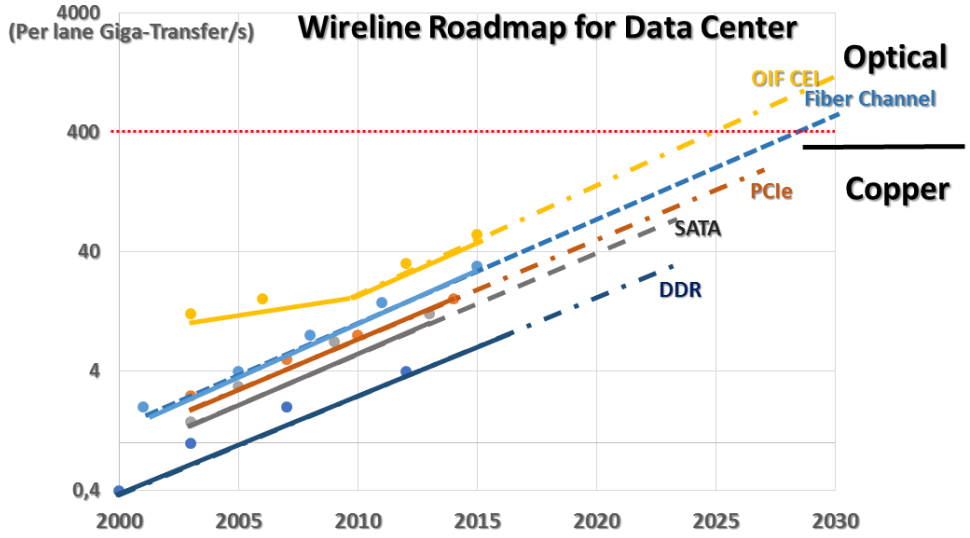
Research Priorities

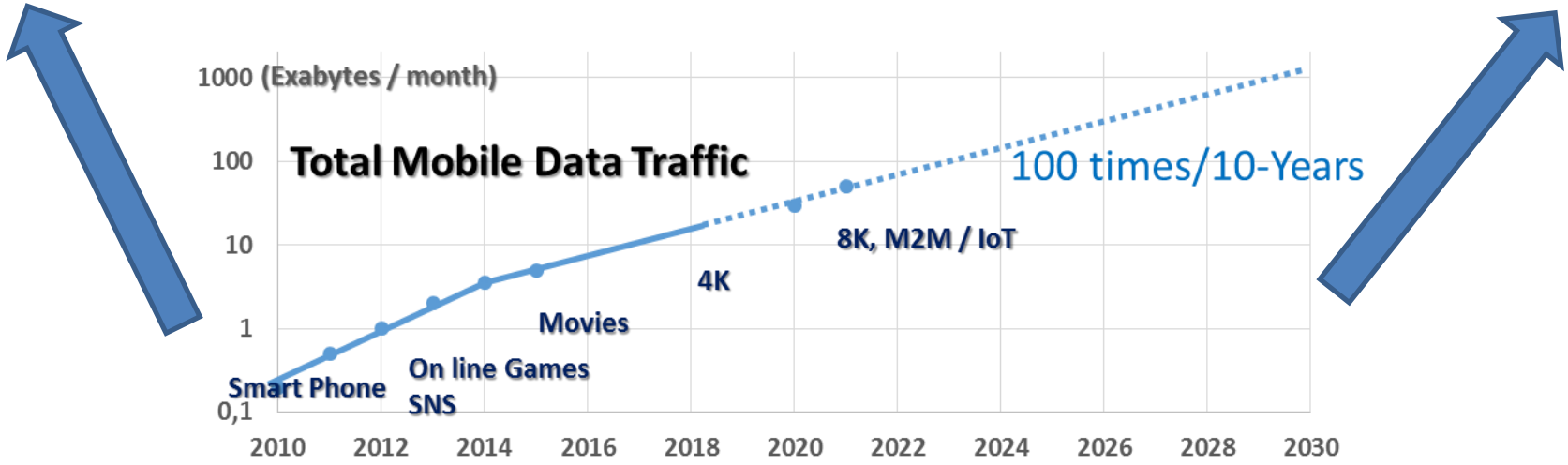
Connectivity (Wireline and Wireless)
(NEREID TASK 3.2)

- The Outdoor Wireless Applications
- The Outdoor Wireline Applications
- The Indoor Wireless Applications
- The Indoor Wireline Applications
- The Device to Device Wireless Applications
- The In Package/Device Photonics Wireline Applications

Connectivity Roadmap

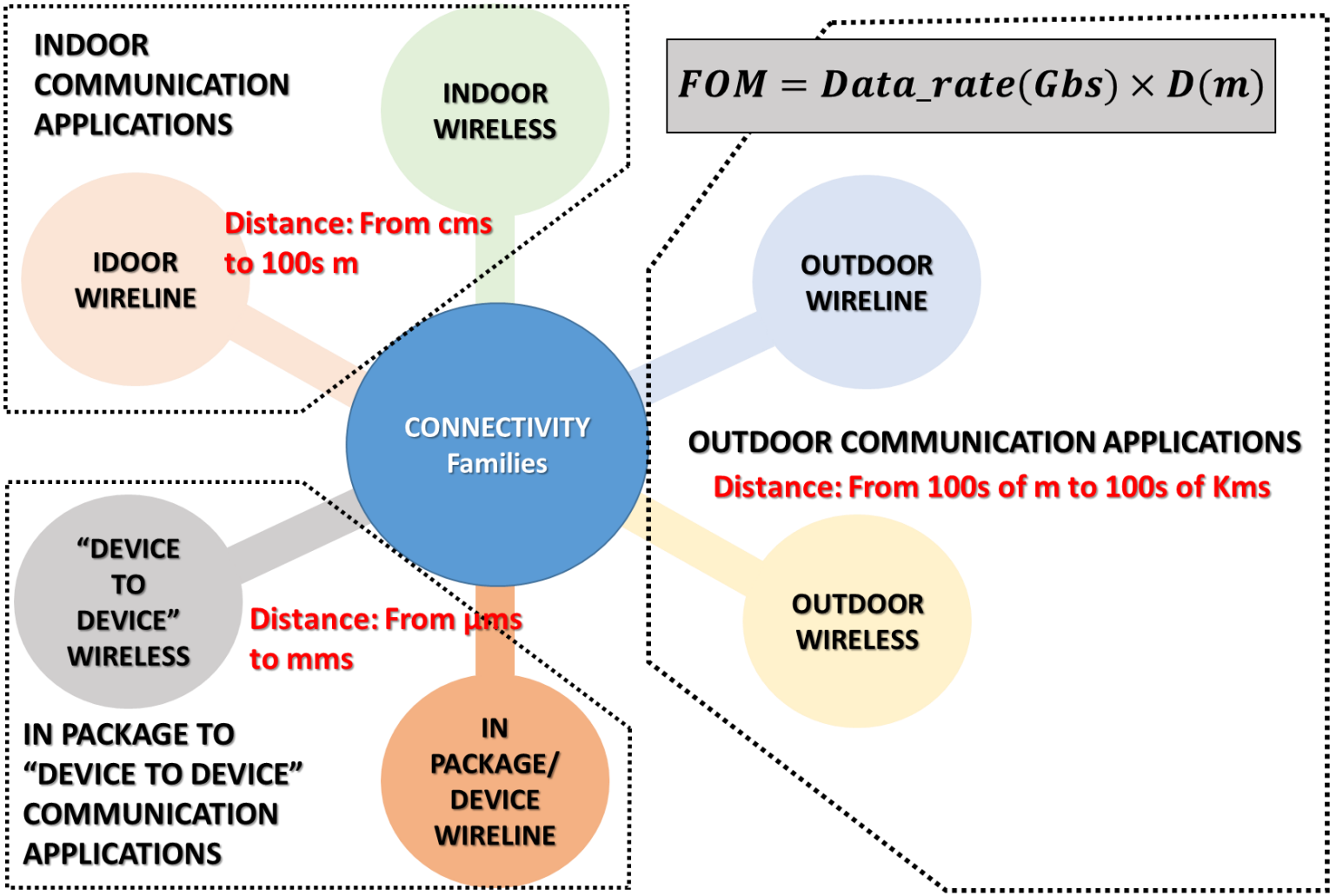




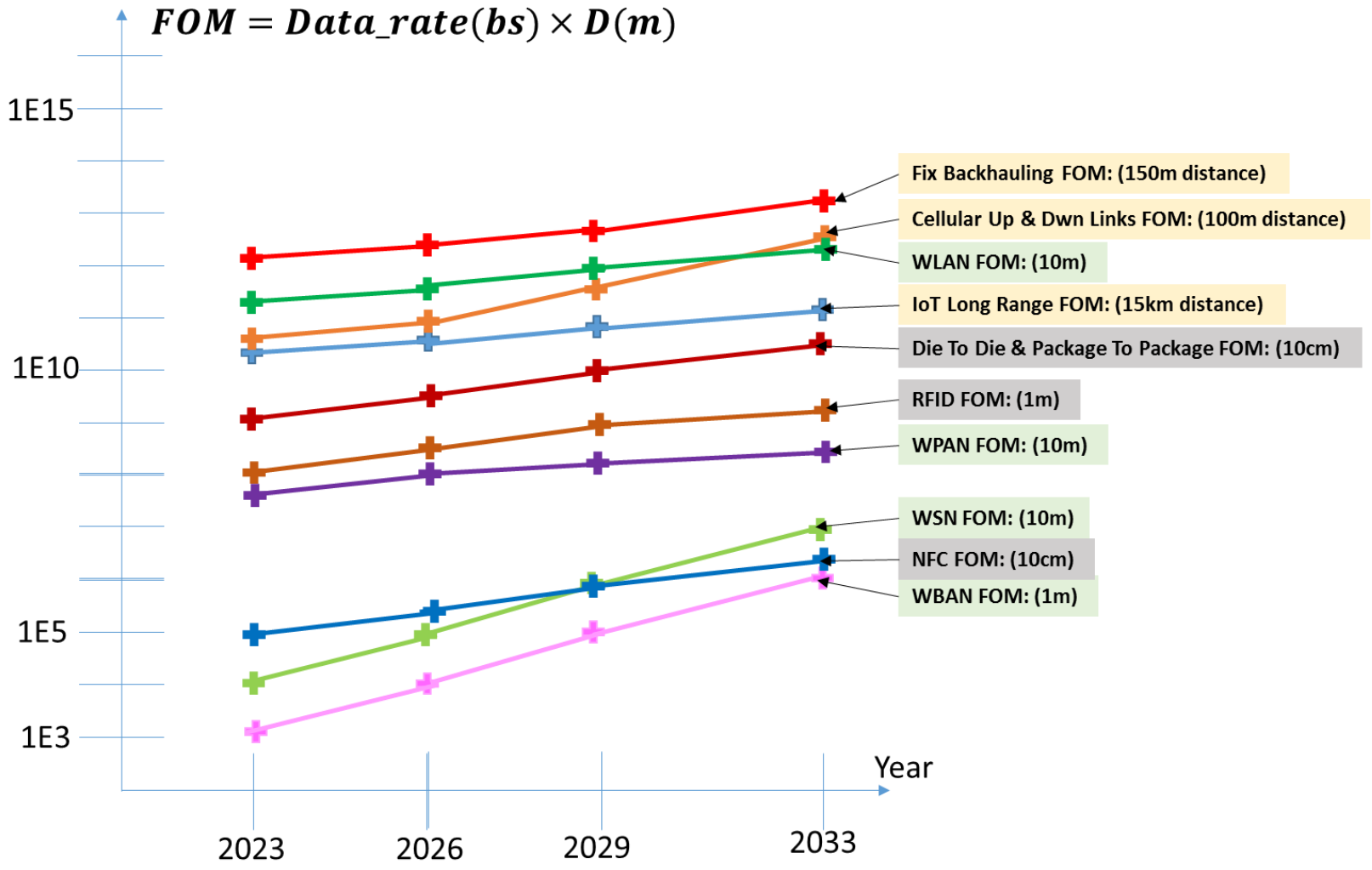


3. Roadmap Building

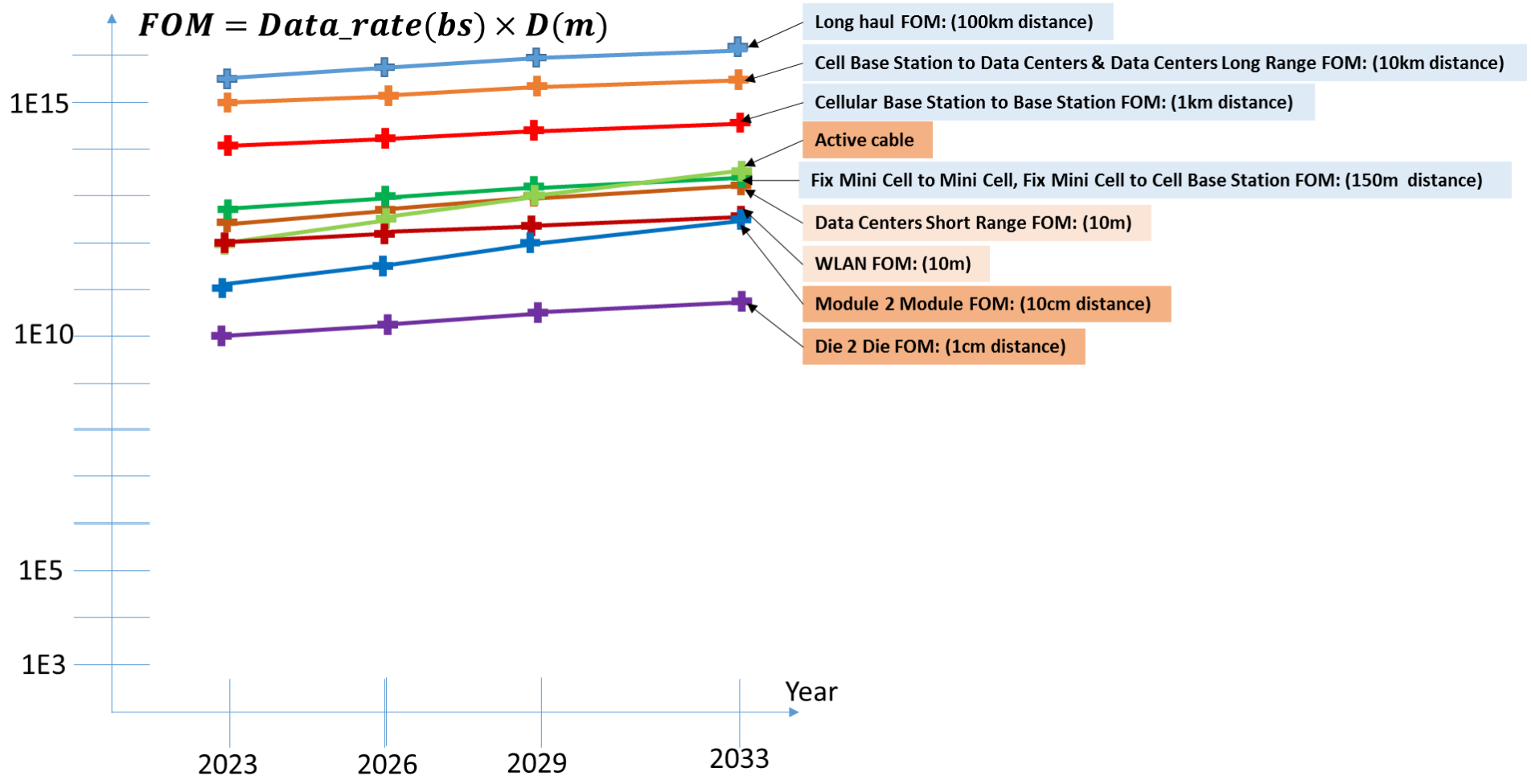
Roadmap Building



3.31 Wireless Connectivity-FOM



3.32 Wireline Connectivity-FOM



Functional Diversification
Smart Sensors

Research Priorities

Smart Sensors (NEREID TASK 4.1)

Sensors for Automotive applications:

-Sensors for navigation and car's basic system performance

*Motion Sensors

*Pressure Sensors

-Advanced drive assistance systems (ADAS) for autonomous cars

*Images Devices

*Radar Sensor

-Pollution/Air quality monitoring based on gas sensors

Sensors for medical and healthcare applications:

-Physiological Signal Monitoring

-Implantable sensors: Bionics

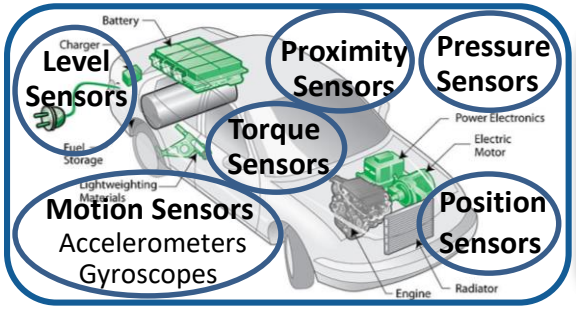
-Molecular Diagnostics

Smart Sensors - Roadmap

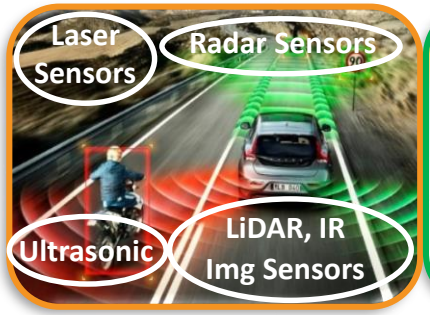
Automotive

sensors to *reduce pollution, energy consumption and to improve safety & security*

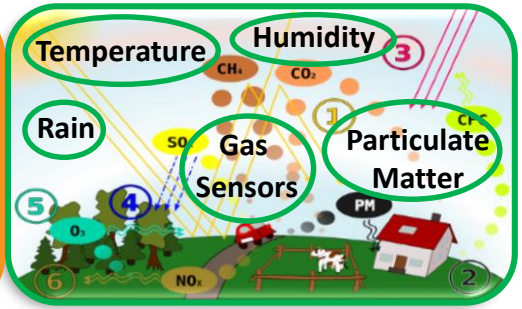
Automotive performance sensors: Inertial and motional sensors



Advanced Driver Assistance System: ADAS



Environmental monitoring : Pollution & Climate status



- Improve accuracy
- Share manufacture infrastructure costs with other applications

Medical and healthcare

sensors are developing very fast.

Applications

- Drug Development
- Patient Monitoring
- Clinical Operation
- Clinical Imaging
- Fitness & Wellness

Devices

mHealth
Wearable Sensors

Bionics
Implantable Sensors

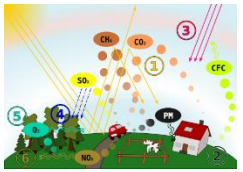
Molecular diagnosis

End Users

- Patients
- Biotech companies
- Research labs of pharma
- Healthcare providers & players
- Government authority

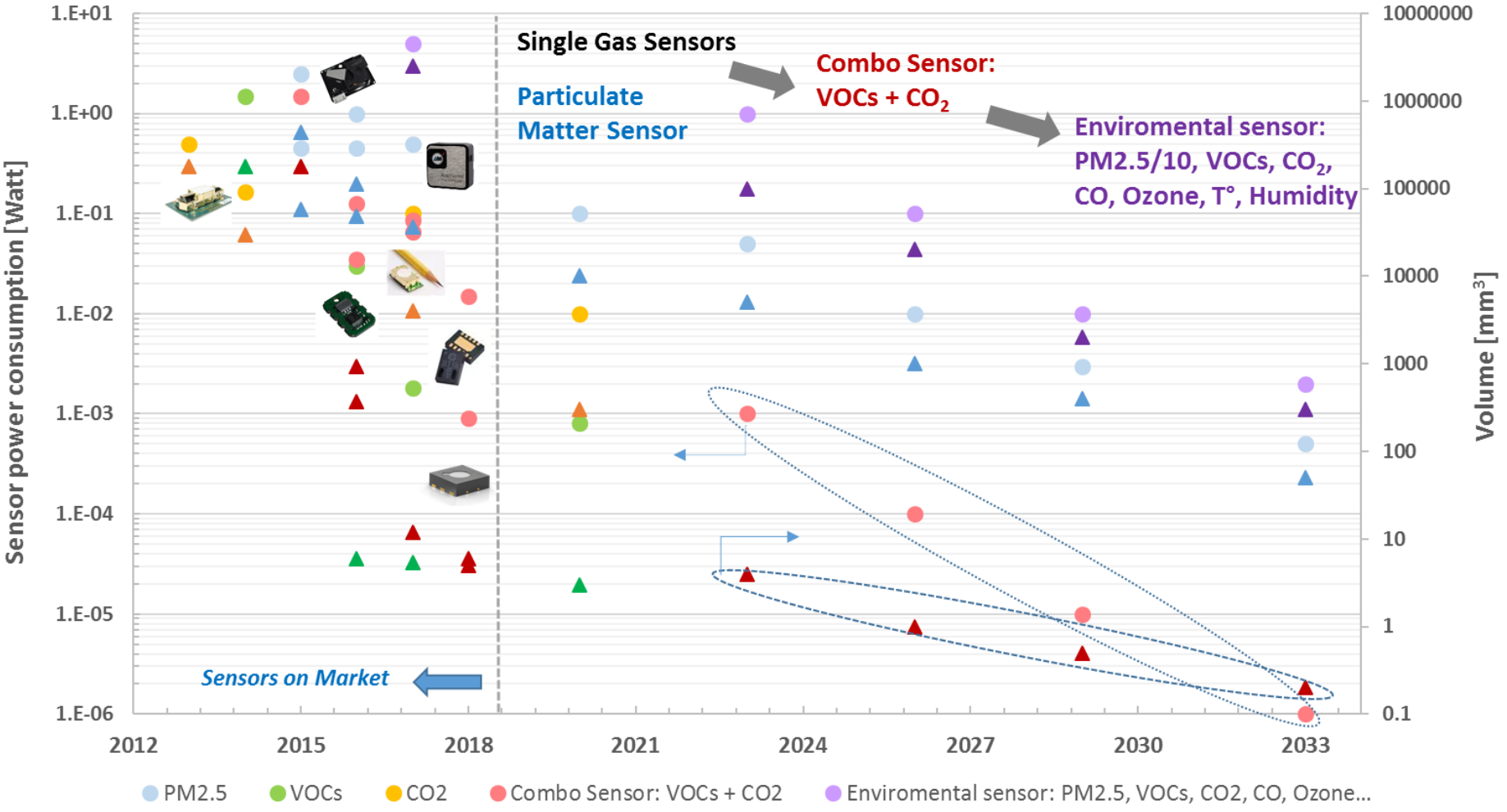
- Cost and convenience (for the patient, the hospital, etc.)
- Long and tedious development stage

Pollution/Air quality monitoring with gas sensors



Gas Sensor: NO_2, O_3 , CO, SO_2

Particulate Matter Detection: PM2.5 and PM 10



Highlights of Smart Sensors

Healthcare and automotive are of **high relevance for European industry and research**. In this sectors **quality** is even more important than the **price.**

- **Well-penetrated healthcare systems**
- Dominates the **autonomous vehicle market** with major technology manufactures and early commercialization of **ADAS systems**.

Some of the smart sensor identified gaps by 2030 concern: ***manufacturability and cost*** *(hybrid integration),* ***low power consumption*** *(energy efficiency, zero-power or self-powered sensors),* ***robustness*** *(stability) of design and in production* ***reliability****.*

- **Lack of metrology & standards:** clinical validation, FDA approvals…
- **Lack of regulations:** reduce emissions, dependence in oil…
- **Auto-calibration** or self-calibrated sensors
- Sensor packaging, compatibility and CMOS integration
- **Connected objects** and Internet of things (IoT)
- **Sensor Fusion/** Wireless Sensor Network (WSN)

Sensors relevant in other segments:
- consumer electronics: **motion MEMS**
- industrial: **image sensors**
- infrastructure: **air quality sensors**
- defense: **LiDAR**
- etc.

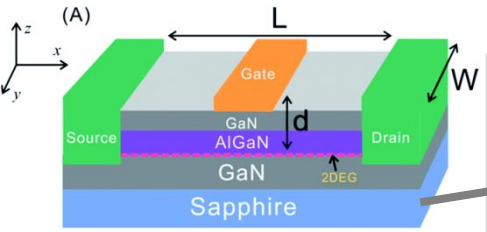
Functional Diversification
Smart Energy

Research Priorities

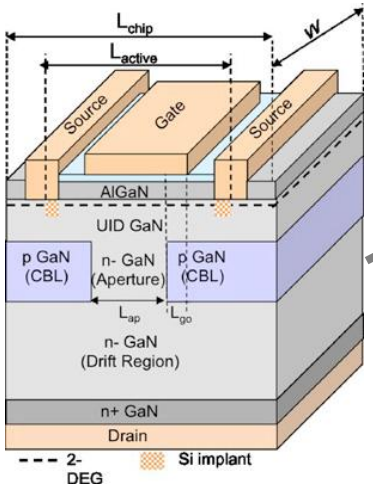
Smart Energy
(NEREID TASK 4.2)

- Si based power devices
- GaN-devices and substrates
- SiC-based substrates
- Alternative Wide Bandgap Semiconductors: AlN, Ga_2O_3, Diamond

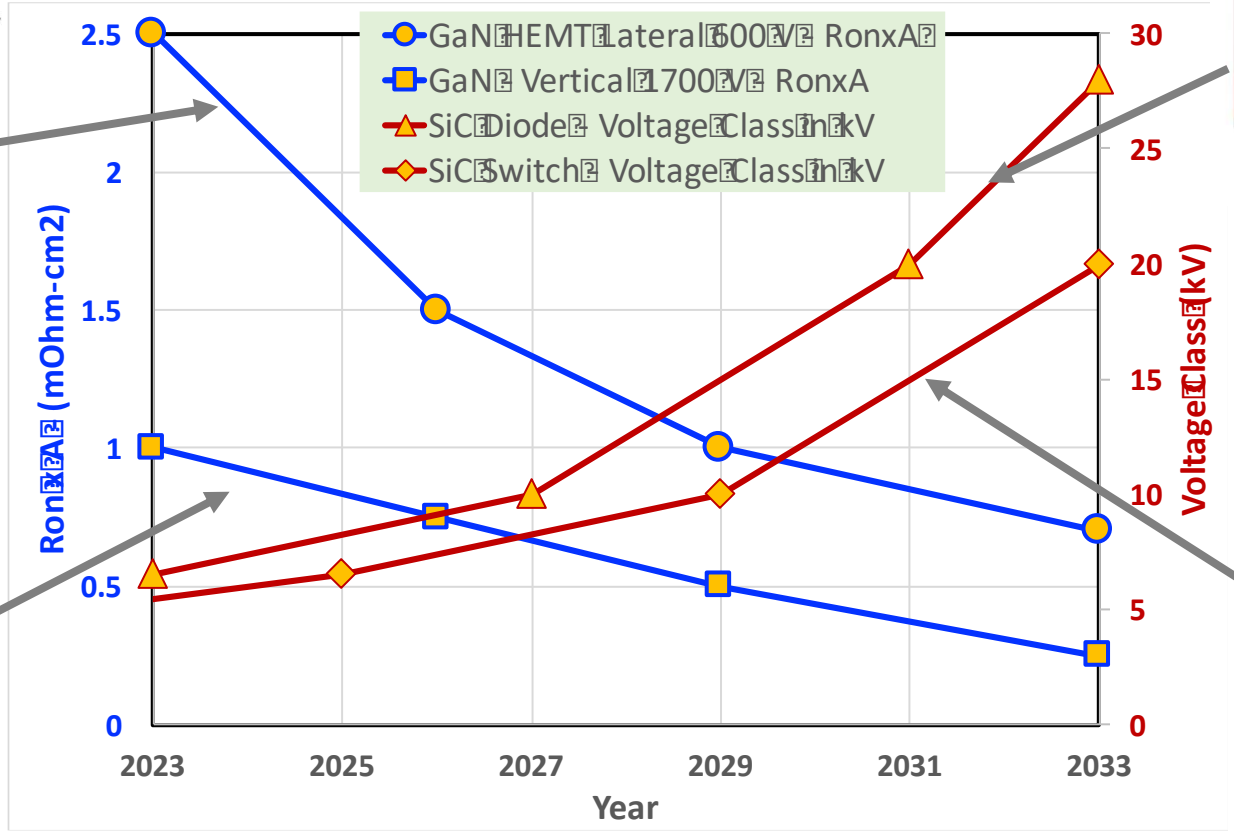
Smart Energy - Roadmap



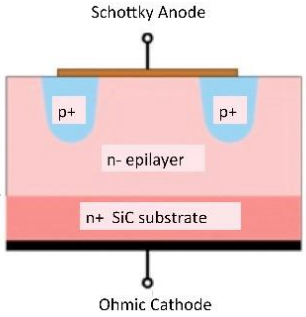
GaN HEMT (Lateral)



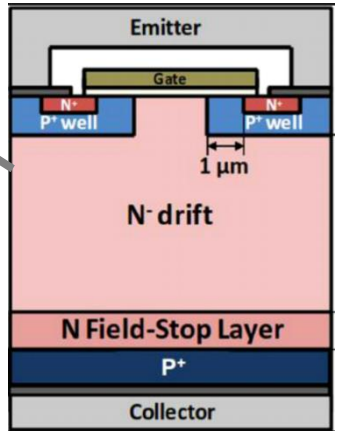
GaN Vertical



GaN/SiC Roadmap



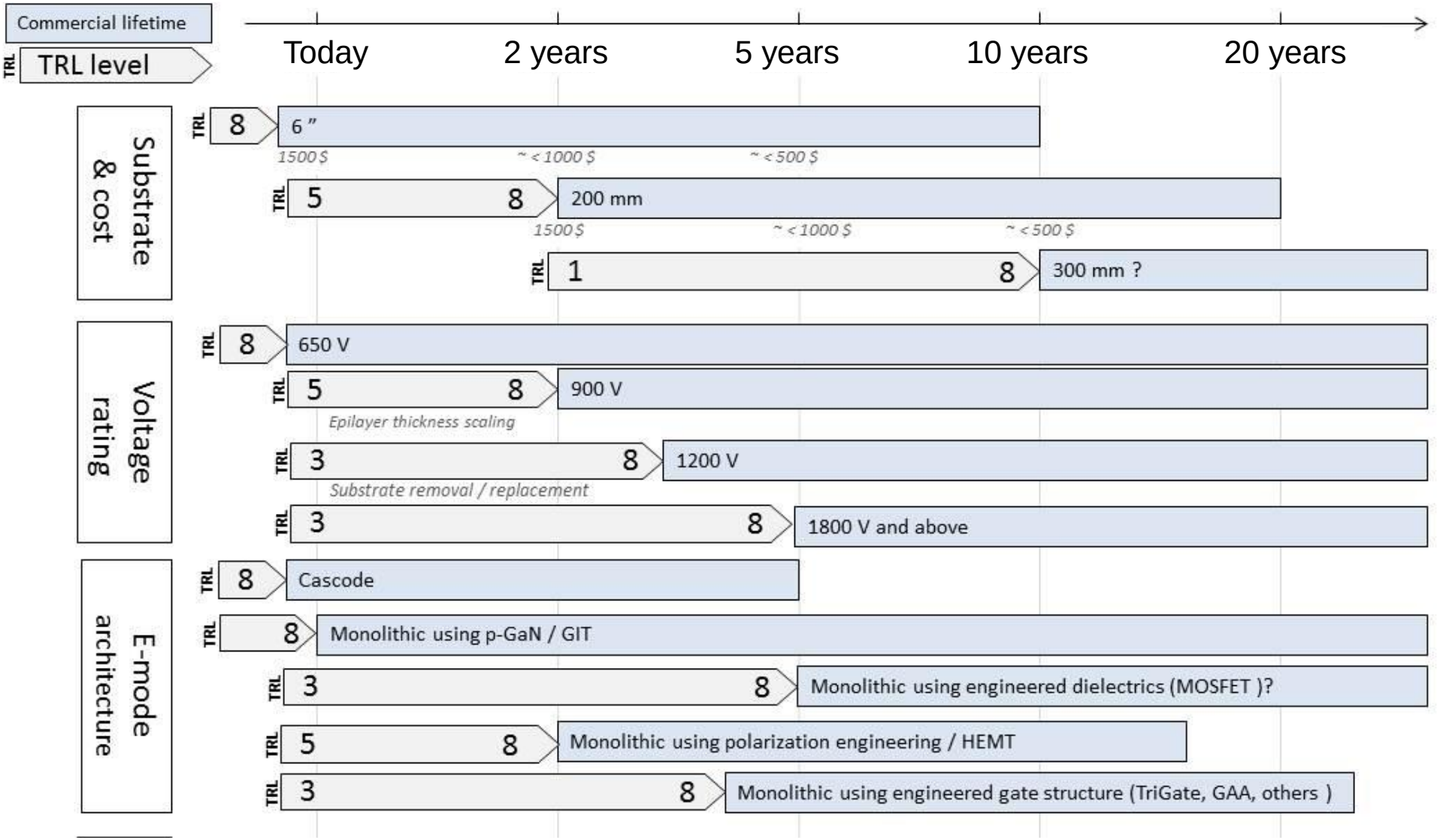
SiC Diode



SiC Switch

Smart Energy - Roadmap

➢ *GaN-on-Si Roadmap*



Smart Energy devices open issues

- **Fast switching is the key for size and weight reduction** with WBG power semiconductors leading to several issues:
  EMC, low parasitic inductances of the **packaging** and interconnection technologies, power losses related to **passive** components, need for system **integration solutions**, optimized switching cell, integrated drivers, ...

- As a consequence, the extreme miniaturization of power electronic systems leads to **higher power density** which requires **new improved cooling techniques**, but also leads to higher operation (and junction) temperature.

- **Issues related to high temperature power electronics**:
  advanced materials and processes for **packaging** and interconnection (chip level and system level), polymer moulding & encapsulation, substrates, temperature range for passive components, **robustness** and reliability.

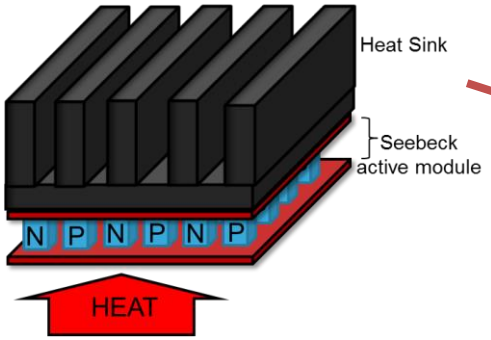
Functional Diversification
Energy for autonomous systems

Research Priorities

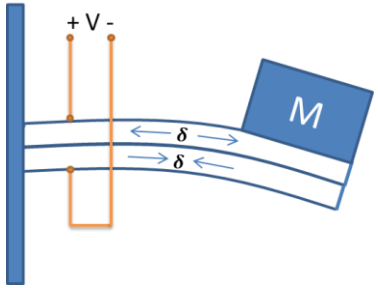
Energy for Autonomous Systems
(NEREID SubTASK 4.2.1)

- Mechanical EH: Electrostatic transduction
- Mechanical EH: Piezoelectric transduction
- Mechanical EH: Electromagnetic transduction
- Thermal energy harvesting
- Photovoltaic Energy Harvesting
- RF energy harvesting/wireless power transfer
- Energy storage - Microbatteries
- Energy storage - Microcapacitors
- Micro-Power Management

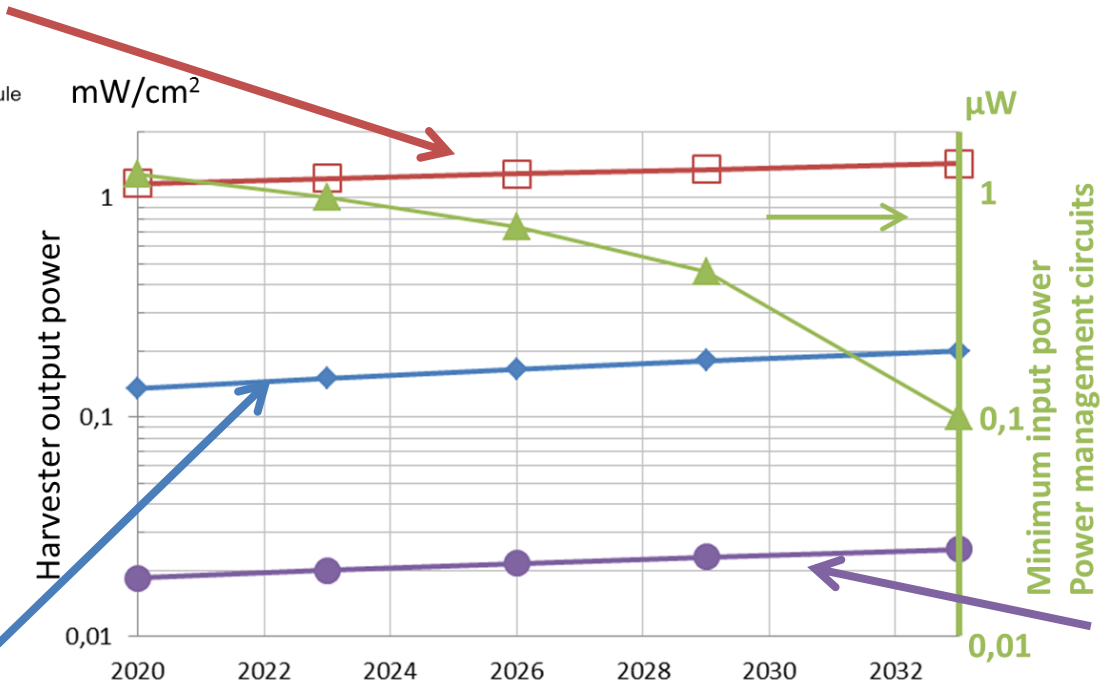
Energy for autonomous systems - Roadmap



Thermoelectric generators



MEMS Piezogenerators

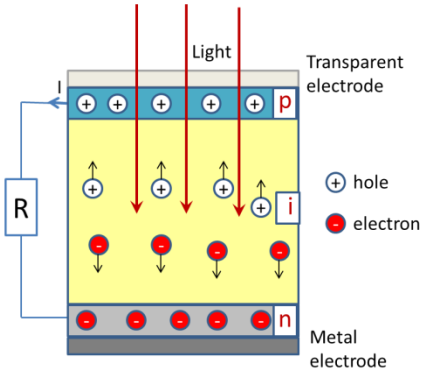


MEMS piezogenerators (<300Hz,<0,5G)

Thermoelectric generators (based on ΔT≈2.3K, 40µm thick thermoelectric module, mm scale heat sink)

Indoor solar cells (300Lux)

Power management circuits



Solar cells

Highlights of Energy for autonomous systems

- IoT and energy harvesting are application-driven today, so projects should mainly focus on the development of a complete application (from harvesting to the use case)
- The improvement of energy harvesters performance and efficiency is as important as the development of “green” materials.
- The use of nanotechnologies is foreseen to increase the performance of all the concepts in general.
- Increasing the bandwidth at a low frequency target (below 100Hz) will help to fit applications for vibration based mechanical energy harvesters.
- Power management circuits key issues: inductors size reduction, develop planar alternatives to inductors, reduce leakages.

System Design
and
Heterogeneous Integration

Research Priorities

System Design and Heterogeneous Integration (NEREID Workpackage 5, WP5)

In this chapter, the main concepts are classified by connecting the three applications

- Automated Driving;
- Implantable Devices;
- Environmental Monitoring and Wearable Systems,

with different elements of Application-Aware Hardware-Software-Co-Design. These Elements comprise Functionalities, Implementation Qualities and Criticalities and Needs.

Equipment, Materials and Manufacturing Science

Research Priorities

Equipment and Manufacturing Science
(NEREID Workpackage 6, WP6)

- More Moore
- More-than-Moore
- Manufacturing Science

Thank you !

Download the NEREID Roadmap at https://www.nereid-h2020.eu/roadmap

Download the IRDS Roadmap at **https://irds.ieee.org/**

Contact : francis.balestra@grenoble-inp.fr