



“NOMODAC” PROJECT : MINI WORKSHOP

Time domain NOise MOdeling for circuit Design cycle ACceleration

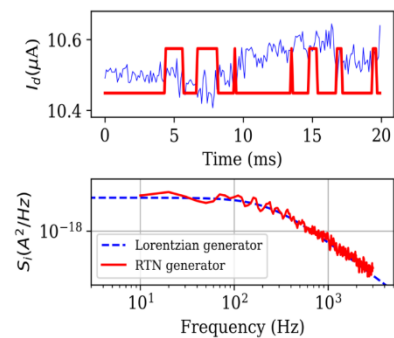


April 15th 9:30-12:00 @ Salle Belledonne / CROMA lab

The NOMODAC project

The goal of the NOMADAC project is to address the issue of delay in the circuit design cycle, related to time-domain noise simulations, by proposing solutions of noise modeling methods and tools that can significantly accelerate the simulation time of noise-aware circuit design. Taking advantage of UGA’s expertise in transistor noise modeling and AUTH’s (Aristotle University of Thessaloniki) experience with circuit noise and automated circuit design, a variety of methods for time domain noise modeling will be explored, along with different model implementations (Verilog-A and C) in circuit simulations. All types of electronic noise will be considered: thermal, flicker (1/f), generation-recombination (g-r) and random telegraph noise (RTN). The developed method’s performance will be benchmarked against already existing ones, for circuits like VCOs, Mixers, ADCs (Analog-Digital) and DACs (Digital-Analog Converters).

This mini-workshop aims to present the project’s vision and the relevant research activities of the CMNE (CROMA) and ASIC Lab (AUTH) teams, followed by a presentation of some preliminary project results and peripheral activities of the DHREAMS (CROMA) team.



[Tataridou et al., IEEE Journal of the Electron Devices Society, 2022]

PROGRAM

Overview

- 9:30 - Opening / Introduction of the NOMODAC project** (Dr. Christoforos THEODOROU - project coordinator from CROMA)
- 10:00 - Relevant research activities of AUTH ASIC Lab** (Prof. Thomas NOULIS - project partner from AUTH)
- 10:30 - Relevant research activities of CMNE team** (Dr. Christoforos THEODOROU - project coordinator from CROMA)
- 11:00 - Relevant research activities of DHREAMS team** (Dr. Pietro FERREIRA - invited colleague)
- 11:30 - Preliminary results and challenges** (Panagiota FASILI - internship student from AUTH)

Detailed program

10:00 - Relevant activities of AUTH ASIC Lab (Aristotle University of Thessaloniki)

This talk focuses on the recent research activities of AUTH ASIC LAB of Aristotle University of Thessaloniki over the past five years. The work centers on analog and mixed-signal integrated circuit design, with emphasis on low-power operation, high-frequency performance, and noise-aware techniques for RF and mmWave applications. Particular attention is given to emerging methodologies that incorporate machine learning into electronic design automation, enabling faster and more efficient circuit optimization. The presented work highlights the

convergence of microelectronics and data-driven design approaches toward next-generation, high-performance, and energy-efficient systems.

Prof. Thomas Noulis is an Associate Professor in the Physics Dept. of Aristotle Univ. of Thessaloniki, Greece and the



Head of the ASIC Lab team, and a Semiconductor Industry expert (INTEL Corp., INFINEON AG, HELIC Inc. (acquired by ANSYS)) with more than 15 years of international experience in Design System Development, Analog/RFMS circuit Design, Design Methodology and international project management. He holds B.Sc. Degree in Physics (2003), MSc. Degree in Electronics Engineering (2005), and a Ph.D. (2009) from Aristotle Univ. of Thessaloniki (collaboration with LAAS, Toulouse-France). He is the main author of more than 100 publications, holds one European patent and the Editor/ co-editor of five books. He is an active reviewer and a member of the editorial board of international scientific journals and conferences. His research interests are focused on Low noise circuit design, Signal and Power Integrity, Design Methodology and sensor interfaces.

10:30 - Relevant research activities of CMNE team (CROMA)

This talk will summarize all the recent research activities of CMNE team concerning the frequency and time-domain noise modeling approaches for nano-scale MOSFET noise effects such as Lorentzian and Random Telegraph Noise. A short introduction will also be made on the basic physical mechanisms behind these types of noise and the importance of modeling them for accurate circuit simulations, using the Verilog-A behavioral language.

Dr. Christoforos Theodorou holds B.Sc. Degree in Physics (2006), MSc. Degree in Electronics Engineering (2008), and a



Ph.D. (2013) from Aristotle Univ. of Thessaloniki. After working as a post-doc researcher in academia and an electronics engineer in industry, he is, since 2017, a CNRS Researcher at the CROMA laboratory, Grenoble, France. His main research focuses on the characterization, modeling and simulation of noise and variability effects in novel nano-scale devices (SOI FETs, ReRAMs, 2D, III-V..) and circuits, with a more recent interest on cryogenic electronics. He is the author/co-author of 67 journal articles, 47 communications in International Conferences and 1 book chapter, a TPC member for the ESSERC, ULIS/EUROSIOI and MOCASST conferences, and member of the steering committee in the International Conference on Noise and Fluctuations (ICNF).

11:00 - Preliminary results and challenges

This short talk will talk about some preliminary scientific output obtained thanks to the work of the intern student Panagiota Fasili, exploring different ideas of time-domain modeling for thermal, flicker and gate noise.



Panagiota Fasili is an internship Master student from Aristotle Univ. of Thessaloniki (AUTH), working in CROMA on the characterization and modeling of noise phenomena in ultra-scaled transistor devices. She holds B.Sc. Degree in Physics (2024) from AUTH.

11:30 - Noise-Optimized Neuromorphic Spiking Radio in Context-Aware IoT (CROMA)

To bring Artificial Intelligence on the edge of Internet of Things sensing, this work aims an RF neuromorphic spiking radio which is noise optimized to operate under stochastic resonance in weak inversion. The proposal is neuromorphic spiking radio using noise-optimized eNeurons.

Prof. Pietro FERREIRA (IEEE S'03-SG'06-M'12-SM'18) received the B.Eng. cum lauda in Electronics and Computer Eng. in



2006, the M.Sc. in Microelectronics in 2008 from the Federal University of Rio de Janeiro (UFRJ), Brazil, the Ph.D. degree in Communications and Electronics in 2011 from the Télécom Paris (IPP), France, and Research Direction Diploma (HDR) in Physics in 2019 from the Université Paris-Saclay, France. Researching high-performance high-reliability circuits and systems, he joined IM2NP lab. (UMR CNRS 7334) for one year and IEMN lab. (UMR CNRS 8520) for two years during his tenure track. From 2014 to 2024, he was Associate Professor at Université Paris-Saclay, CentraleSupélec, GeePs (UMR CNRS 8507). Since 2024, he is Full Professor at Université Savoie Mont-Blanc, CROMA (UMR CNRS 5130). His research interests are design methodologies and microwave instrumentation techniques for ultra-low power integrated circuits in harsh environments. Recent projects aim the Internet of Things industry considering IA-edge and reliability.