Low temperature semiconductor layer transfer for 3D sequential integration:
materials physics and electrical performances

The fabrication of integrated circuits with multiple stacked transistor layers, or sequential 3D integration, allows for ultra-dense vertical connectivity, tackling wire delay problems and increase the number of transistors per unit area without requiring costly feature size reduction. A major challenge for 3D sequential integration is that it requires limiting the thermal budget of top layer devices processing to ensure the stability of the bottom layer devices. At LETI, we are developing different alternatives to obtain the top Si layer "substrate" at low temperature (LT). To understand the physics and qualify the performances of LT substrates, a pertinent electrical characterization method is needed. With this in mind, we have recently developed a new test vehicle configured as a double-gate pseudo-MOSFET structure (DG-ΨMOSFET [SSE 2021 and INFOS 2021]), and demonstrate the pertinence of this device for parameter extraction of SOI. In another recently accepted communication [VLSI 2021] we report excellent electrical results with advanced devices integrated on a first generation of LTSOI. These preliminary studies set the basis for the thesis. The work will rely on two major aspects: (i) deliver a complete understanding of the new DG-ΨMOSFET device behavior and adapted electrical parameters extraction, and; (ii) use the electrical vehicle, and complementary physical characterization methods, to understand the materials physics for 3D substrate level integration and its compatibility with devices integration.

The work is organized such as the fabrication and physical characterization of the substrates and devices will be done in CEA-LETI. The electrical characterization of the devices will be done in IMEP-LaHC.

CEA-LETI, in Grenoble, capital of the french alps, is an institute dedicated to applied research in micro- and nano-technologies, information technologies and technologies for healthcare. LETI is the privileged interface between industry and academia. Through research programs using worl-leading technology patforms, it ensures the development and industrial transfer of innovative technologies in a wide range of sectors.

IMEP-LaHC, is a « unité mixte de recherche » (CNRS / Grenoble INP / UGA / Université Savoie Mont Blanc) of 110 people strongly committed in research activities related to micro- and nano-electronics, microphotonics, micro- and nano-systems, microwaves and microwave-photonics.

Requested skills: the candidate must have good knowledge on semiconductor materials and device physics, an experience on technological process, on electrical parameter extraction is a plus. She/he must be curious, self-motivated and autonomous, in order to fully benefit from this collaborative thesis in a highly technological environment.

Contacts: Shay Reboh (Shay.REBOH@cea.fr) and Irina Ionica (Irina.Ionica@grenoble-inp.fr)