Recent Publications

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July 2017

Selection of recent Publications in **International Journals**

Yong Xu, T. Minari, K. Tsukagoshi, R. Gwoziecki, R. Coppard, F. Balestra, J.A. Chroboczek, G. Ghibaudo
Extraction of low-frequency noise in contact resistance of organic field-effect transistors,
APPLIED PHYSICS LETTERS **97**, 033503, 2010

Yong Xu, R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra, and G. Ghibaudo
Modified transmission-line method for contact resistance extraction
in organic field-effect transistors
APPLIED PHYSICS LETTERS 97, 063302, 2010

Y. Xu, T. Minari, T. Kazuito R. Gwoziecki, F. Balestra, J.A. Chroboczek, G. Ghibaudo
Diagnosis of low-frequency noise sources in contact resistance of staggered organic transistors
APPLIED PHYSICS LETTERS **98**, 033505, 2011

Yong Xu, Takeo Minari, Kazuhito Tsukagoshi, Jan Chroboczek, Francis Balestra, G. Ghibaudo
Origin of low-frequency noise in pentacene field-effect transistors
Solid State Electronics **61**, 106 (2011)

Y. Xu, F. Balestra, G. Ghibaudo,
Theoretical analysis of carrier mobility in organic field-effect transistors,
Applied Physics Letters, Vol. 98, no. 23, art. no. 233302 (Jun 2011)

Y. Xu, T. Minari, K. Tsukagoshi, R. Gwoziecki, R. Coppard, M. Benwadih, J. Chroboczek, F. Balestra, G. Ghibaudo
Modeling of static electrical properties in organic field-effect Transistors
JOURNAL OF APPLIED PHYSICS 110, 014510 (2011)

I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, P. Perreau, A. Margain, F. Boeuf, F. Balestra, G. Ghibaudo
Characterization and modelling of capacitances in FD-SOI devices
Solid-State Electronics, 2011

Y. Xu, T. Minari, R. Gwoziecki, F. Balestra, G. Ghibaudo
Power transfer-length method for full biasing contact resistance evaluation of organic field-effect transistors
Organic Electronics, Vol 12 , 2019-2024 (2011)

Yong Xu, Mohamed Benwadih, Romain Gwoziecki, Romain Coppard, Takeo Minari, Chuan Liu, Kazuhito Tsukagoshi, Jan Chroboczek, Francis Balestra, and Gerard Ghibaudo
Carrier mobility in organic field-effect transistors
J. Applied Physics 110, 104513, 2011

I.Ben Akkez, C.Fenouillet-Beranger, A.Cros, P.Perreau, S.Haendler, O.Weber, F.Andrieu, D.Pellissier-Tanon, F.Abbate, C. Richard, R. Beneyton, P. Gouraud, A. Margain, C. Borowiak, E. Gourvest, K.K.Bourdelle, B.Y.Nguyen, T.Poiroux, T.Skotnicki, O.Faynot, F.Balestra, G.Ghibaudo, F.Boeuf
Study of substrate orientations impact on Ultra Thin Buried Oxide (UT BOX) FDSOI high-k Metal gate technology performances
Solid State Electronics, to be published (2012)

Yong Xu, William Scheideler, Chuan Liu, Takeo Minari, Francis Balestra, Gerard Ghibaudo, and Kazuhito Tsukagoshi
Contact Thickness Effects in Bottom-Contact Coplanar Organic Field-Effect Transistors

IEEE Electron Dev. Lett., vol. 34, p. 535, April 2013

Yong Xu, Chuan Liu, Yun Li, Peter Darmawan, Takeo Minari, Francis Balestra, Gerard Ghibaudo and Kazuhito Tsukagoshi
Joule's law for organic transistors exploration: case of contact resistance
J. Appl. Phys. **113**, 064507 (2013)

K. Bennamane, I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, F. Balestra and G. Ghibaudo
Mobility coupling effects due to remote Coulomb scattering in thin film FD-SOI CMOS devices
Electronics Letters, 2013

Yong Xu, Chuan Liu, William Scheideler, Peter Darmawan, Songlin Li, Francis Balestra, Gerard Ghibaudo, Kazuhito Tsukagoshi
How small the contacts could be optimal for nanoscale organic transistors?
Organic Electronics
Volume 14, Issue 7, July 2013, Pages 1797–1804

Yong Xu, William Scheideler, Chuan Liu, Songlin Li, Francis Balestra, Gerard Ghibaudo, Kazuhito Tsukagoshi
Understanding Thickness Dependent Charge Transport in Pentacene Transistors by Low-Frequency Noise
IEEE Electron Device Letters (2013)

Yong Xu, Chuan Liu, Huabin Sun, Francis Balestra, Gerard Ghibaudo, Will Scheideler, Yong-Young Noh
Metal evaporation dependent charge injection in organic transistors,
Organic Electronics 15, 1738–1744 (2014)

Francis Balestra, Gérard Ghibaudo, Jalal Jomaah,
Noise in advanced MOSFETs and Beyond-CMOS devices"
Invited Paper, Special Issue on "Noise modeling of high-frequency semiconductor devices", Wiley "International Journal of Numerical Modelling: Electronic Networks, Devices and Fields", 28, pp. 613-627 (2015)

Yong Xu , Chuan Liu, Paul Seyram K. Amegadze, Won-Tae Park Dang Xuan Long, Takeo Minari, Francis Balestra, Gerard Ghibaudo, and Yong-Young Noh
Significant roles of low-temperature post-metallization annealing in solution-processed oxide thin-film transistors
Applied Physics Letters **105**, 133505 (2014)

F. Balestra
Multi-Gate Devices, Nanowires and Small Slope Switches for very low energy consumption and new functionalities
Invited paper, IOP Publishing, Journal of Physics, Volume 558, to be published (2014).

F. Balestra
Challenges to Nano-scale Device World
Invited paper, ECS Transactions (2015)

Yong Xu, Chuan Liu, Paul Seyram K. Amegadez, Gi-Seong Ryu, Huaixin Wei, Francis Balestra, Gerard Ghibaudo, and Yong-Young Noh
On the Origin of Improved Charge Transport in Double-Gate In–Ga–Zn–O Thin-Film Transistors: A Low-Frequency Noise Perspective

ELECTRON DEVICE LETTERS, VOL. 36, NO. 10, OCTOBER 2015

L. Gaben, S. Barraud, M.-P. Samson, M.-A. Jaud, S. Martinie, O. Rozeau, J. Lacord, C. Arvet,

C. Vizioz, J. Bustoss, J.-A. Dallery, S. Pauliac, V. Balan, C. Euvrard, C. Perrot, V. Loup, P. Besson, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet

Evaluation of Stacked Nanowires Transistors for CMOS: Performance and Technology Opportunities
Invited paper, ECS Transactions, to be published (2016)

F. Balestra, G. Ghibaudo,

Physics and performance of nanoscale semiconductor devices at cryogenic temperature **Review paper**, Semiconductor Science and Technology, https://doi.org/10.1088/1361-6641/32/2/023002 (2016)

Adam Dobri, Simon Jeannot, Fausto Piazza, Carine Jahan, Jean Coignus, Luca Perniola,

Francis Balestra,

Development and application of the Oxide Stress Separation technique for the measurement of ONO leakage currents at low electric fields in 40 nm floating gate embedded flash memory, Microelectronics Reliability, Vol. 69 (2017)

Selection of recent Publications in **International Conferences**

J. Jomaah, K. Bennamana, F. Balestra, G. Ghibaudo
Low temperature characterization of different deep submicron SOI and FinFET devices
WOLTE'9, Guaruja, Brazil, June 2010

Yong Xu, Gérard Ghibaudo, Francis Balestra, Jan Chroboczek, Romain Gwoziecki, Isabelle Chartier, and Romain Coppard
Static and low frequency noise characterization of P-type polymer and N-type small Molecule OFETs, ICOE'2010, Paris, June 2010

F. Balestra
Silicon-based devices and materials for nanoscale FETs,
Invited paper, 6th International SemOI Conference & 1st Ukrainian-French Seminar on SOI Materials, Devices and Circuits, Kiev, October 2010, Proceedings p. 11

Y. Xu, T. Minari, T. Kazuito R. Gwoziecki, F. Balestra, J.A. Chroboczek, G. Ghibaudo
Analysis of Low Frequency Noise in Organic Field Effect Transistors Combining Static and Noise Data,
ICNF'2011, Toronto, June 2011

I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, P. Perreau, A. Margain, F. Boeuf F. Balestra, G. Ghibaudo
Characterization and Modeling of Capacitances in FD-SOI Devices
ULIS'2011, Cork, Ireland, March 2011

Francis Balestra
Fundamental scientific challenges and limits for very low energy computation
Invited paper, FET11, Budapest, May 2011

Y. Xu, G.Ghibaudo, F. Balestra, M. Benwadih, R. Gwoziecki, R. Coppard
On the Temperature Dependence of Carrier Mobility in Organic Transistors
ICOE2011, Roma, Italy, 2011

I.Ben Akkez,C.Fenouillet-Beranger, A.Cros, P.Perreau, S.Haendler, O.Weber, F.Andrieu, D.Pellissier-Tanon, F.Abbate,C. Richard, R. Beneyton, P. Gouraud, A. Margain, C. Borowiak, E. Gourvest, K.K.Bourdelle, B.Y.Nguyen, T.Poiroux, T.Skotnicki,O.Faynot, F.Balestra, G.Ghibaudo, F.Boeuf
Impact of substrate orientation on Ultra Thin BOX Fully Depleted SOI electrical performances
ULIS 2012, Grenoble, March 2012

I.Ben Akkez, C.Fenouillet-Beranger, A.Cros, P.Perreau, S.Haendler, O.Weber, F.Andrieu, D.Pellissier-Tanon, F.Abbate, C. Richard, R. Beneyton, P. Gouraud, A. Margain, C. Borowiak, E. Gourvest, K.K.Bourdelle, B.Y.Nguyen, T.Poiroux, T.Skotnicki, O.Faynot, F.Balestra, G.Ghibaudo, F.Boeuf
Impact of 45° rotated substrate on UTBOX FDSOI high-k metal gate technologies
VLSI-TSA, Taiwan, April 2012

I.Ben-Akkez, C.Fenouillet-Beranger, A. Cros, P. Perreau, F. Balestra ,G. Ghibaudo, F. Boeuf
Low temperature mobility study in UTBOX FD SOI devices: Rotated versus not rotated Substrate

EuroSOI 2012, Montpellier, Jan. 2012

F. Balestra
Challenges and limits for very low energy computation
Invited paper, FTM'2012, Corsica, June 2012

F. Balestra
New devices and materials for ultra low power operation
Invited paper, ICMNE'2012, Moscow, October 2012

F. Balestra
Challenges and limits for very low energy computation
Invited paper, ICSICT'2012, Xi'An, China, October 2012

I.Ben-Akkez, C.Diouf, A. Cros, C.Fenouillet-Beranger, P. Perreau,
F. Balestra, G. Ghibaudo, F. Boeuf
On the understanding of mobility degradation mechanisms in advanced CMOS devices: FDSOI versus bulk technology
SSDM'2012, Kyoto, Japon, Sept. 2012

Imed Ben Akkez, Antoine Cros, Claire Fenouillet-Beranger, Frederic Boeuf,
Quentin Rafhay, Francis Balestra, Gérard Ghibaudo
New Parameter Extraction Method Based on Split C-V for FDSOI MOSFETs
ESSDERC'2012, Bordeaux, Sept. 2012

F. Balestra,
Challenges and solutions for very low energy computation
Invited paper, 7th International Workshop "Functional Nanomaterials and devices" and 2nd Ukrainian-French Seminar "SOI Materials, devices and circuits: Physics, Technology and diagnostics", Kiev, April 2013

F. Balestra
Alternative materials and Beyond-CMOS FETs for very low power operation
Invited paper, CMOS-ETR Symposium, July 2014, Grenoble

F. Balestra
Ultra low power device operation
Invited paper, Conference Nano and Giga challenges in Electronics, Photonics and Renewable Energy, March 2014, Phoenix, Arizona

F. Balestra
Nanowires for very low power ICs and new functionalities
Invited paper, World Congress of Nano Science &Technology (Nano-S&T 2013), Xi'an, China, Sept. 2013

F. Balestra
Challenges and solutions for very low energy consumption
Invited paper, International Symposium Component Base of Silicon Micro- and Nanoelectronics and Solid-State Quantum Computers, Moscow, Sept. 2013

I.Ben-Akkez, C. Fenouillet-Beranger A.Cros, F.Balestra, G. Ghibaudo
Evidence of mobility enhancement due to back biasing in UTBOX FDSOI high-k Metal gate technology
2013 IEEE S3S Conference, Oct. 2013

F. Balestra, G. Ghibaudo, M. Mouis, J. Jomaah, I. Ben-Akkez
Physics of semiconductor devices at cryogenics temperature
Invited paper, WOLTE10 (10th International Workshop On Low Temperature Electronics), Paris, Oct. 2013

I. Ben-Akkez, C. Fenouillet-Beranger , A. Cros, F. Balestra, G. Ghibaudo
Impact of back biasing on the effective mobility in UTBB FDSOI CMOS technology
ISCDG 2013, Dresden, Germany, Sept. 2013

F. Balestra

Challenges and solutions for very low energy consumption
Invited paper, PIEZO'NEMS'2013, Grenoble, Nov. 2013

F. Balestra
Multi-Gate Devices, Nanowires and Small Slope Switches for very low energy consumption and new functionalities
Invited paper, ISCMP "Challenges of Nanoscale Science: Theory, Materials, Applications" Varna, Bulgaria, Sept. 2014

F.Balestra
Fully-depleted SOI MOSFETs, Multi-Gate Devices, Nanowires and Small Slope Switches for very low power operation
Invited paper, Nano S&T, Qingdao, Chine, Oct. 2014

F. Balestra
Alternative materials and beyond-CMOS FETs for very low power operation
Invited paper, ICMNE'2014, Moscou, Oct. 2014

F. Balestra
Invited paper, Nanowires for ultimate CMOS and Small Slope Switches,
Emerging Technologies Symposium, Vancouver, May 2015

F. Balestra
Invited paper, Challenges to Nano-scale Device World
Int. Symposium on Advanced CMOS-Compatible Semiconductor Devices XVII, ECS Meeting, Chicago, May 2015.

L. Gaben, S. Barraud, M.-P. Samson, J.-M. Hartmann, C. Vizioz, F. Aussenac, F. Allain, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet
P-type Trigate Nanowires: Impact of Nanowire Thickness and Si0.7Ge0.3 Source-Drain Epitaxy
EUROSOI-ULIS'2015, Bologna, Jan. 2015

F. Balestra
Challenges to ultra-low-power operation
Invited paper, FTM'2015, Mallorca, Spain, June 2015

F. Balestra
Novel Materials for Ultimate Nanoelectronic Devices
Invited paper, WCSM 2016, Singapour, March 2016

F. Balestra
New Materials and Innovative Architectures for Ultimate Nanoelectronic Devices
Invited paper, CMOS ETR 2016, Montreal, May 2016

L. Gaben, S. Barraud, P. Pimenta-Barros, Y. Morand, J. Pradelles, M.-P. Samson, B. Previtali, P. Besson, F. Allain, S. Monfray, F. Bœuf, T. Skotnicki, F. Balestra, and M. Vinet
Ω-Gate Nanowire Transistors Realized by Sidewall Image Transfer Patterning with a 35nm pitch and opportunities for stacked-Nanowires architectures, SSDM 2015, Sapporo, Septembre 2015 ***(SSDM Young researcher Award)***

Loïc Gaben, Sylvain Barraud, Marie-Anne Jaud, Sébastien Martinie, Olivier Rozeau, Joris Lacord, Gaspard Hiblot, Stéphane Monfray, Frédéric Bœuf, Thomas Skotnicki, Françis Balestra, Maud Vinet
Stacked-Nanowire and FinFET Transistors: Guidelines for the 7nm node, SSDM 2015, Sapporo, Septembre 2015

F. Balestra
Emerging Steep Switch Devices & CMOS technologies for ultra low power operation
Invited Paper, Perspectives in Nano Information Processing, Cambridge, 14-16 December 2015

Adam Dobri, Simon Jeannot, Fausto Piazza, Carine Jahan, Jean Coignus, Luca Perniola,

Francis Balestra
Oxide Stress Separation technique for the assessment of inter-gate dielectric integrity in 40nm Flash memory cells, SISC 2015, Arlington, Dec. 2015

L. Gaben, S. Barraud, M.P. Samson, M.-A. Jaud, S. Martinie, O. Rozeau, J. Lacord, C. Arvet, C. Vizioz, J. Bustoss, J.-A. Dallery, S. Pauliac, V. Balan, C. Euvrard, C. Perrot, V. Loup, P. Besson, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet
Evaluation of Stacked Nanowires Transistors for CMOS: Performance and Technology Opportunities, **Invited paper**, ECS 2016, San Diego, USA, May 2016

F. Balestra
NanoCMOS and Steep Switch Technologies for Ultimate Nanoelectronics Devices, **Invited paper**, ICSICT'2016, Hangzhou, China, Oct. 2016

F. Balestra
Innovative Nanodevices for the end of the roadmap: Ultimate scaling, power and performance**, Invited Paper**, ISCMP "Advances in Nanostructured Condensed Matter: Research and Innovations", Varna, Bulgarie, Sept. 2016

Loïc Gaben, Arthur Arnaud, Marios Barlas, M. P. Samson, C. Arvet, C. Vizioz, J.-M. Hartmann, S. Barraud, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet
Stacked Nanowires FETs: Mechanical Robustness Evaluation for sub-7nm Nodes. Silicon Nanoelectronics Workshop, Honolulu, June 2016

Loïc Gaben, Sébastien Pauliac, Jacques-Alexandre Dallery, Jessy Bustos, Romaric Dechanoz, Beatrice Hemard, Laurent Koscianski, Xavier Bossy, Marie-Pierre Samson Sylvain Barraud, Stéphane Monfray, Frédéric Bœuf, Thomas Skotnicki, Francis Balestra, Maud Vinet
HSQ Lithography for Nanowire First Integration: an Interesting Alternative for Gate Last Fabrication of Sub-7nm Stacked Nanowire FETs, SSDM'2016, Tsukuba, Japan, September 2016

Francis Balestra
Challenges and solutions for high performance nanoscale devices combined with nanomaterials, **Invited paper**, WCSM'2017, Bangkok, March 2017

Francis Balestra
Novel Materials for Low-Power and High-Performance Nanoscale FETs, **Invited paper,** ETCMOS 2017, Warsaw, May 2017

210. Francis Balestra
Ultra low power and high performance nanoelectronic devices, **Invited paper,** IEEE ASICON 2017, Guiyang, China, October 2017

Francis Balestra
NanoCMOS and Tunnel FETs for the end of the Roadmap, **Invited paper**, NGC 2017, Tomsk, Russie, Septembre 2017

Francis Balestra
Innovative materials for nanoscale MOSFETs and Small Slope Switches**, Invited paper**, WSCM 2018, Osaka, Japon, March 2018

Francis Balestra
Ultimate CMOS and Beyond-CMOS for the end of the Nanoelectronic Roadmap, **Invited paper,** Nano S&T 2017, Fukuoka, Japon, Octobre 2017

Francis Balestra
Beyond CMOS-devices and Future of Nanoelectronics**, Invited paper**, NANOFIS 2017, Graz, Autriche, November 2017

Adam Dobri, Dann Morillon, Simon Jeannot, Fausto Piazza,Carine Jahan, Alain Toffoli, Luca Perniola, Francis Balestra, Evaluation of ONO compatibility with high-k metal gate stacks for future embedded flash products, EUROSOI-ULIS 2017, Athènes, Avril 2017

L. Gaben, S. Barraud, V. Balan, C. Euvrard, S. Pauliac, J.-A. Dallery, J. Bustos, R. Dechanoz,

B. Hemard, L. Koscianski, X. Bossy, C. Arvet, C. Vizioz, S. Barnola, C. Perrot, J. Sturm, Y. Exbrayat, N. Daventure, V. Loup, P. Besson, B. Perrin, B. Previtali, M.-P. Samson, S. Monfray, F. Boeuf, T. Skotnicki, F. Balestra, M. Vinet
Hydrogen Silsesquioxane Tri-Dimensional Advanced Patterning Concepts for High Density of Integration in sub-7 nm Nodes, EUROSOI-ULIS 2017, Athènes, Avril 2017

Selection of recent Publications in **Books**

F. Balestra
Silicon-based devices and materials for nanoscale CMOS and beyond-CMOS,
Chapter in "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy",
S. Luryi et al Eds, **Wiley**, 2010.

F. Balestra
Nanoscale CMOS: Innovative Materials, Modeling and Characterization,
Book edited by Francis Balestra (650 p), **ISTE-Wiley**, June 2010

A. Nazarov, J.P. Colinge, F. Balestra, J.P. Raskin, F. Gamiz, V.S. Lisenko, Eds.
Semiconductor-On-Insulator Materials for Nanoelectronics applications
Springer, 2011

F. Balestra
Silicon-based devices and materials for nanoscale FETs
Chapter, **Springer -** Electronics Engineering, in "Semiconductor-On-Insulator Materials for NanoElectronics Applications", 2011

G. Ghibaudo, F. Balestra, S. Deleonibus (Guest Editors)
Special Issue of **European Physical Journal - Applied Physics** "*Materials, Devices and Systems Science, Engineering and Architectures*", 2013

F. Balestra
Challenges and limits for very low energy computation,
Chapter in "Future Trends in Microelectronics, Into the Cross Currents",
S. Luryi et al Eds, **Wiley,** 2013

F. Balestra
Beyond CMOS Nanodevices **1**
Book (tome 1) edited by Francis Balestra, **ISTE-Wiley**, 2014

F. Balestra
Beyond CMOS Nanodevices **2**
Book (tome 2) edited by Francis Balestra, **ISTE-Wiley**, 2014

F. Balestra,
Challenges and solutions for very low energy computation
Chapter, **Springer**, in "Functional Nanomaterials and Devices electronics, sensors and energy harvesting", 2014

F. Balestra, E. Sangiorgi, M. Östling, P.E. Hellström
Nanowires for very low power ICs and new functionalities
Chapter, in "CRC Concise Encyclopedia of Nanotechnology", **CRC Press**,
to be published, 2014

F. Balestra
Silicon-On-Insulator Devices
Chapter in the « **Wiley Encyclopedia of Electrical and Electronics Engineering**", published online, 2014.

A. Nazarov, F. Balestra, V. Kilchytska, D. Flandre (Editors)
"Functional nanomaterials and devices for electronics, sensors and energy harvesting"
Book, **Springer** (2014)

F. Balestra, A. Ionescu
Small Slope Switches
Chapter, ISTE-Wiley, in "CMOS Nanodevices 2", 2014

F. Balestra
Ultra low power device operation

Chapter, Springer, in "Nanoscale Materials and Devices for Electronics, Photonics and Solar Energy ", 2015

F. Balestra

Challenges to ultra-low-power operation

Chapter in “Future Trends in Microelectronics, Journey into the Unknown”, S. Luryi et al Eds, **Wiley,** 2015