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SEMINAIRE EXCEPTIONNEL

(de 13 h à 14 h, salle M 253, PHELMA, Bât. INP, Minatec,
ouvert à tous : enseignants, étudiants, chercheurs, administratifs, techniciens)

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"Future of Logic Nano CMOS Technology"

by Prof. Hiroshi IWAI (Tokyo Institute of Technology, Japan),
IEEE-ED Distinguished Lecturer

Abstract: Although Si MOSFETs have dominated the integrated circuit applications over the past four decades, it is anticipated that the development of CMOS would reach MOSFET downsizing limits sometime after the next decade. However, there are no promising candidates which can replace CMOS with better performance for high-density integration with low cost for the moment. Thus, maybe, we have to stick to the CMOS devices until its end. In order to pursue the downsizing of CMOS for another decade, the development of new technologies is becoming extremely important. Not all the companies can necessarily develop the most advanced technology timely and the competition between the leading semiconductor manufacturing companies becomes very severe for their survive. The current status of the frontend of the technologies is as follows: Because of the difficulty in the lithography and also in the I_{on}/I_{off} ratio control, the rate of the shrinkage for the line pitch and gate length becomes significantly less aggressive so that we will face the downsizing limit later than expected before. New device structures such as multi-gate (FinFET, Tri-gate, and Si-nanowire MOSFETs) and FD (Fully Depleted) SOI are replacing conventional planar MOSFETs. Continuous innovation of High-k/metal gate technologies has enabled EOT scaling down to 0.9 – 0.8 nm in production, however, introduction of new materials are desirable for further EOT scaling. In order to decrease the gate length of MOSFETs down to deep sub-10 nm, we have to solve very difficult problems, significant increase in subthreshold current, significant decrease in conduction for small fin width multigate, ultra-thin Si SOI and small EOT high-k MOSFETs, significant increase of gate leakage current and reliability degradation for small EOT MOSFETs, and through-put decrease for very fine lithography. At this moment, we do not know the solutions for those problems, although there are many good challenges in emerging technologies. In this seminar, past, now, and future of logic MOS LSI technologies are explained.

Hiroshi Iwai *received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo and worked in the research and development of integrated circuit technology for more than 25 years in Toshiba. He is now a professor for 15 years of Frontier Research Center and Dept. of Electronics and Applied Physics, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Yokohama, Japan. Since joining Toshiba, he has developed several generations of high density static RAM's, dynamic RAM's, logic LSI's and RF devices including CMOS, bipolar, and Bi-CMOS. He has also been engaged in research on device physics, process technologies, and T-CAD related to small-geometry MOSFETs and high speed bipolar transistors. He has authored and coauthored more than 1,200 international and domestic journal/conference papers. His current research interests are Nano CMOS, Power and Photovoltaic Devices. Dr. Iwai is, a fellow of IEEE, a fellow of Institute of Electrical Engineers Japan, a fellow of the Japan Society Applied Physics, and a fellow of the Institute of Electronics, Information and Communication Engineers of Japan. He is a recipient of many prize and awards such as IEEE J.J. Ebers Award, IEEE Paul Rappaport Award, Prizes for Science and Technology by the Minister of Education, Japan. He served as the chair and member of many organizations and conference committees such as the president of IEEE Electron Devices Society, and the Director of IEEE Division I.*

Institut de Microélectronique, Electromagnétisme et Photonique
MINATEC, Grenoble-INP, 3 Parvis Louis Neel, CS 50257, 38016 GRENOBLE CEDEX 1, France
Tél. +33 (0) 456.529.503 - Fax. +33 (0) 456.529.501
UMR 5130 CNRS INPG UJF
Institut Polytechnique de GRENOBLE