SEMINAIRE
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"4H-SiC Trenched & Implanted Vertical JFETs (TI-VJFETs)"

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Abstract: SiC JFETs may have the lowest overall losses of switching devices and can operate at temperatures over 400°C. Over different JFET designs the trenched and implanted (TI) gate vertical JFET is very attractive since it may have the lowest on-resistance and its fabrication does not require epitaxial overgrowth or multiple angled ion implantations. The effort for developing high power 4H-SiC JFETs will be presented. Analytical and TCAD modeling, edge termination optimization, lithography approach and device parameter extraction from I-V measurements are some of the issues which will be addressed.

Dr. Konstantinos Zekentes *received his undergraduate degree in Physics, from the University of Crete, Greece, and his Ph.D., in Physics of Semiconductors, from the University of Montpellier, France. He is currently a Senior Researcher with the Microelectronics Research Group (MRG) of the Foundation for Research and Technology-Hellas (FORTH) in Heraklion, Crete, Greece and since April 2016 visiting researcher in IMEP-LAHC. The objective of his work is to coordinate and supervise the MRG's effort for the development of SiC-related technology for elaborating high power/high frequency devices as well as SiC-based 1D devices. Dr. Zekentes has more than hundred seventy journal and conference publications and one US patent.*

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