CMOS Device Scaling: Past, Present, and Future

Date: September 9
Location: Amphi M001, Phelma
Time slot: 10:00am to 11:30am (1h talk & 30 min for questions & open discussion)

Summary:
CMOS technology ushered in the silicon VLSI era over thirty years ago. This talk reviews the history of CMOS devices and projects their future prospects. For any given technology node, CMOS performance is limited by the shortest channel length that can be made while maintaining the integrity of transistor action. The development of the MOSFET scale length theory will be tracked from the 1970s to the present, as it evolves from the one-region model for bulk MOSFETs, to the two-region model for dealing with thick, high-κ gate dielectrics, then to the three-region model for multiple-gate MOSFETs such as FinFETs. It gives powerful guidelines that, along with quantum mechanical considerations, allow the projection of scaling limits for bulk, SOI, double-gate, and nanowire MOSFETs.

Pr. Yuan TAUR short biography

Pr. Yuan Taur received the B.S. degree in physics from National Taiwan University, Taipei, Taiwan, and the Ph.D. degree in physics from University of California, Berkeley.

From 1981 to 2001, he was with the Silicon Technology Department of IBM Thomas J. Watson Research Center, Yorktown Heights, New York, where he was Manager of Exploratory Devices and Processes. Since October 2001, he has been a professor in the Department of Electrical and Computer Engineering, University of California, San Diego. He has been appointed a Distinguished Professor in 2014.

Dr. Yuan Taur was elected a Fellow of the IEEE in 1998. He has served as Editor-in-Chief of the IEEE Electron Device Letters from 1999 to 2011. He has authored or co-authored over 200 technical papers and holds 14 U.S. patents. He co-authored a book with Dr. Tak Ning of IBM, "Fundamentals of Modern VLSI Devices," published by Cambridge University Press in 1998. The 2nd edition was published in 2009.

Dr. Yuan Taur received IEEE Electron Devices Society's J. J. Ebers Award in 2012 "for contributions to the advancement of several generations of CMOS process technologies." He also received IEEE Electron Devices Society's Distinguished Service Award in 2014.