IMEP-LAHC, May 6, 2020

Coupling effects in Monolithic 3D technologies

A LabEX MINOS funded project | Starting year: 2017

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Christoforos THEODOROU (IMEP-LAHC / CMNE) – Co-Supervisor

Outline of Presentation

- Introduction/Motivation
- Device level results
  - Impact of static coupling
  - Impact of dynamic coupling
- Circuit level results
  - Impact of coupling on SRAM, RO
- GP morphology
- Conclusions

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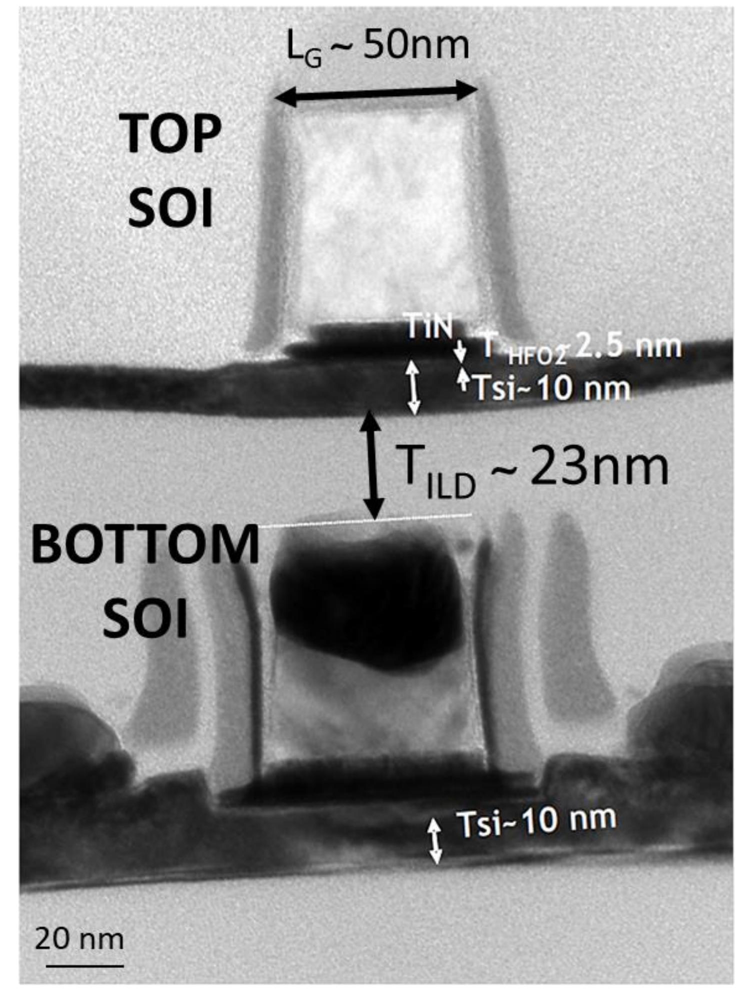
3D Sequential Integration (S3D)

Key advantages

More Moore

- 3DSI vs Planar:
  - -50% area
  - +26% performance/ -20% power



P. Batude et al., IEDM 2011

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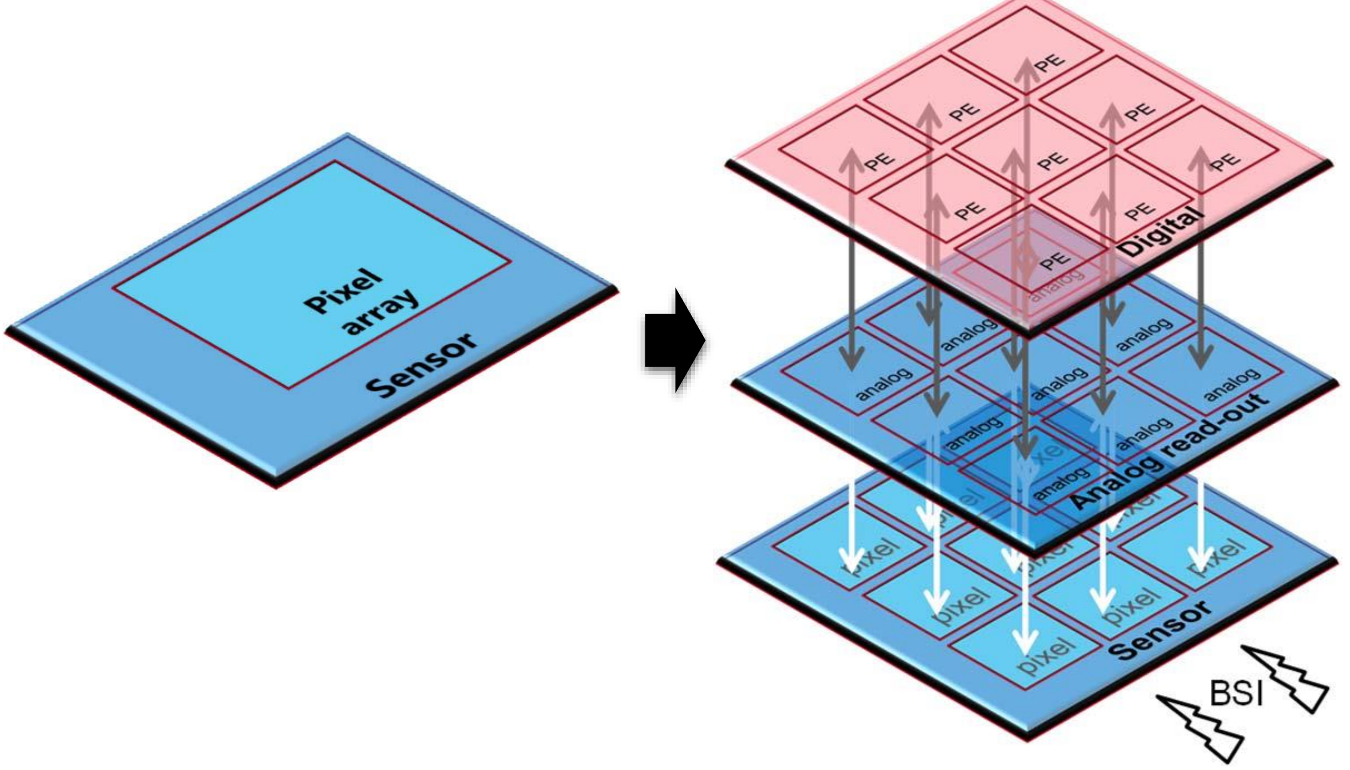
More than Moore

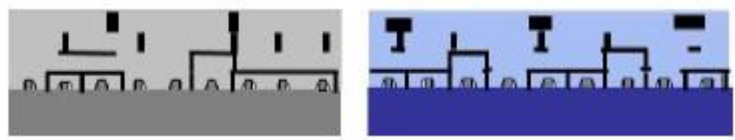
- New functionalities (ex: 3D imagers)



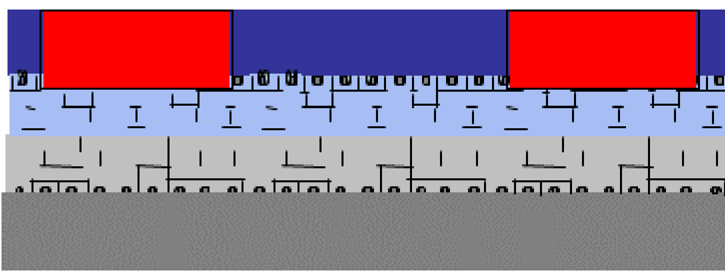
Sequential vs Parallel Integration

Parallel integration
(e.g.: TSV, copper to copper bonding..)

1/ Wafers processed separately

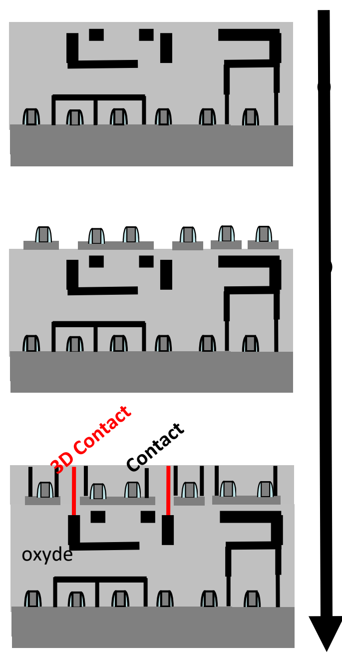


2/ Stacking and contacting



Alignment made during bonding
3σ min = 250nm

Sequential integration

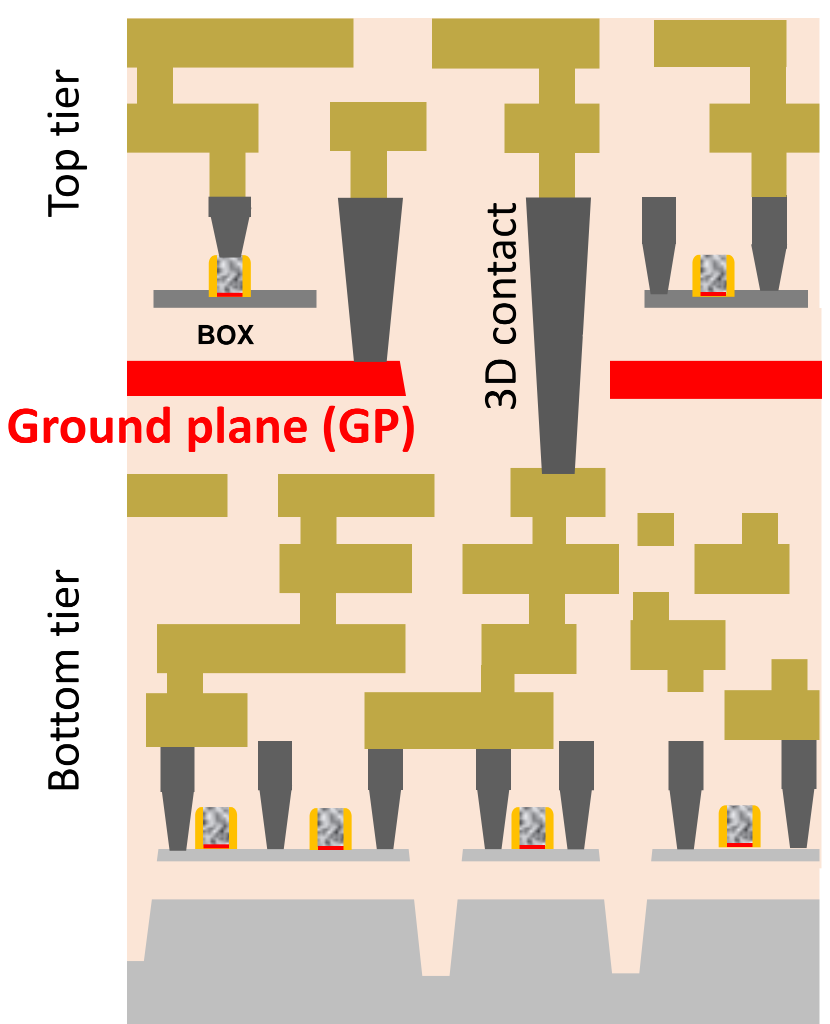


Alignment by lithography
3σ = 5nm (28nm stepper)

3D Sequential Integration (S3D)

Characteristics

- Very thin active & inter-tier layers
- Intermediate back-end-of-line (iBEOL)
- Ground Plane (GP)



3D Sequential Integration (S3D)

Characteristics

- Very thin active & inter-tier layers
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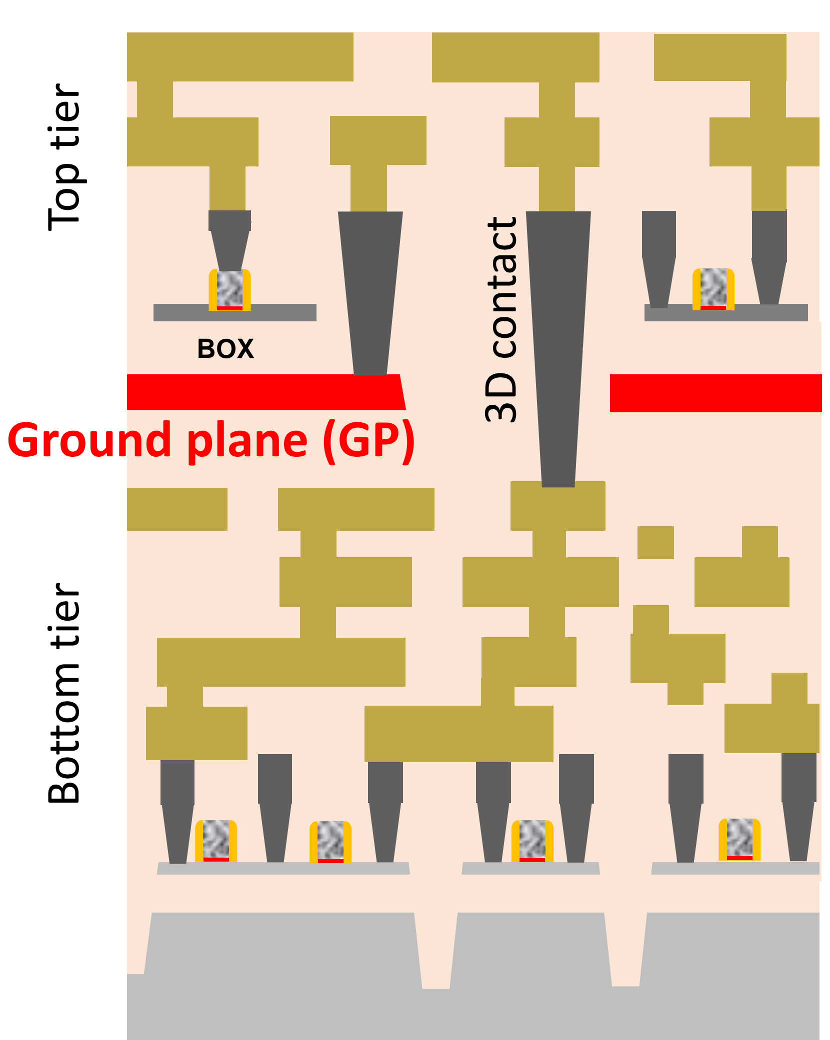
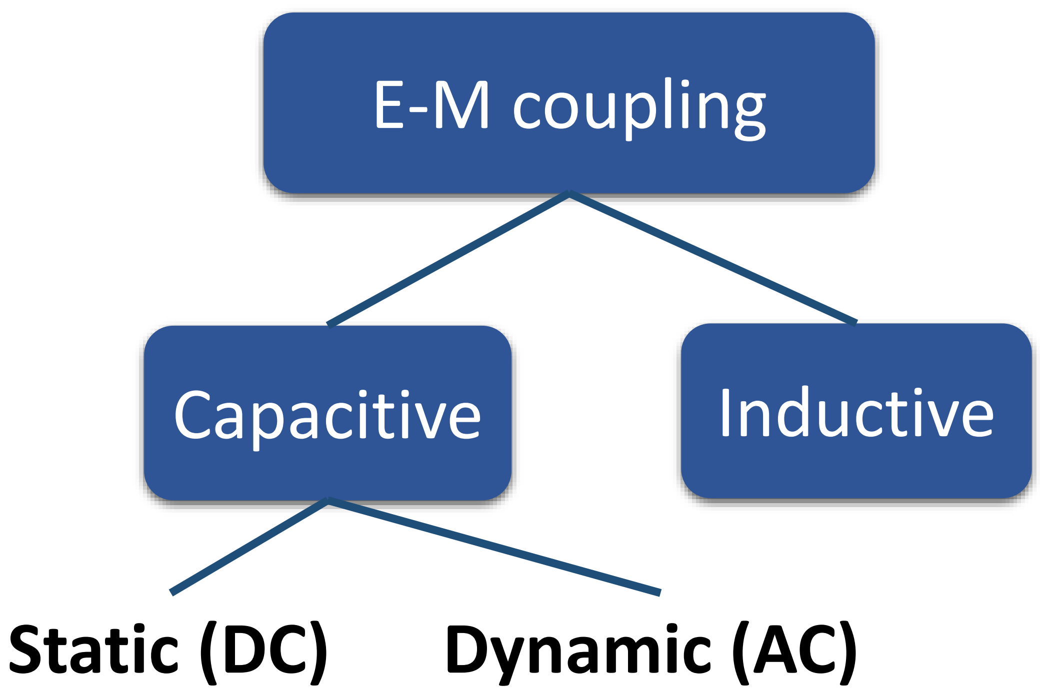
- Ground Plane (GP)

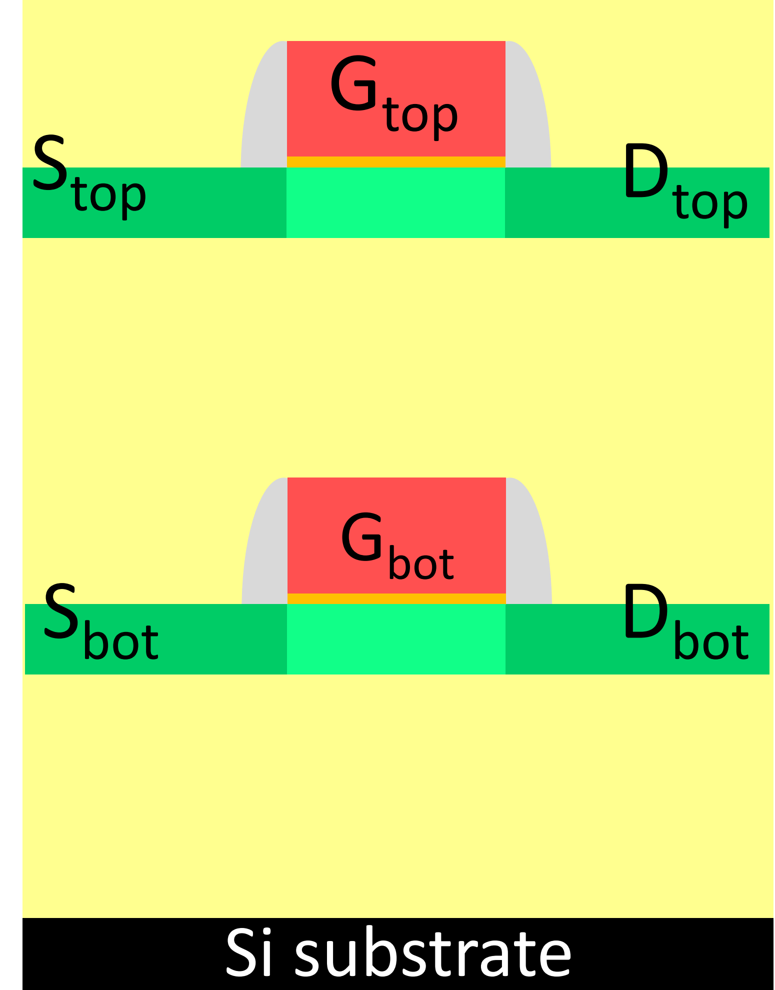
Challenges

- Thermal Budget (TB) constraints
- **Inter-tier coupling between devices**



Inter-tier coupling





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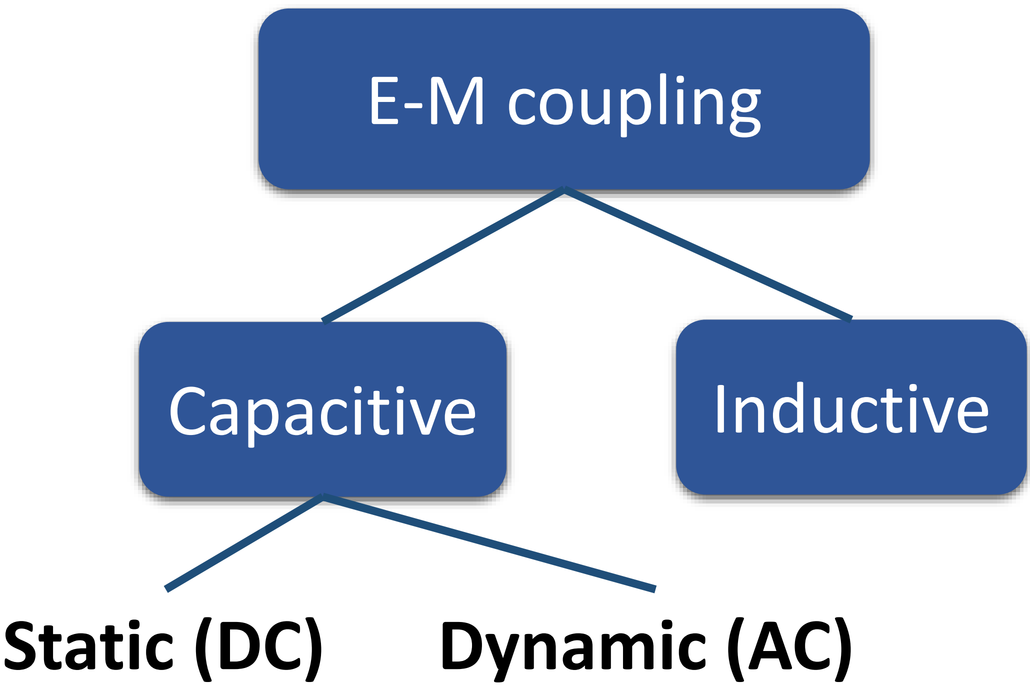
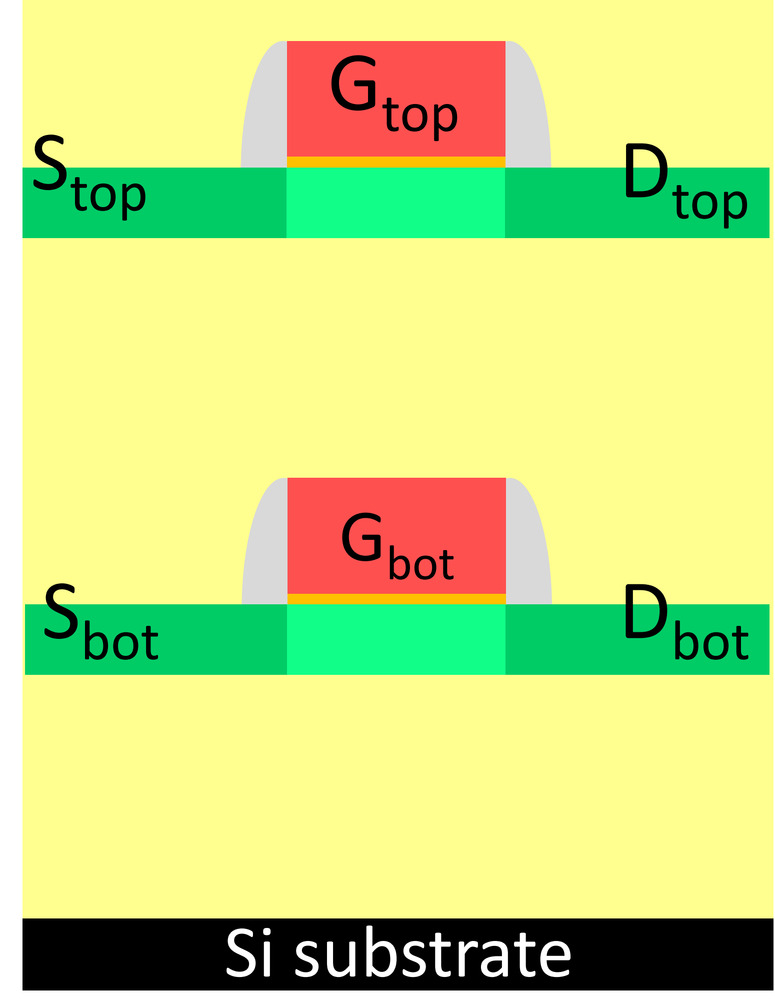
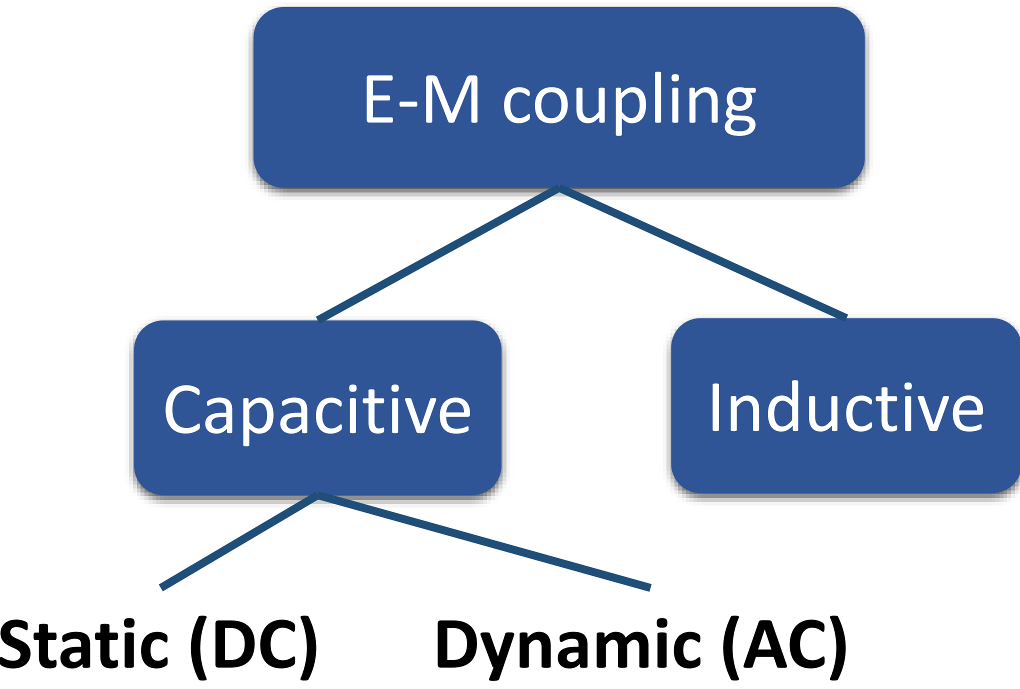




- Identify victim-aggressor pairs
- Relate coupling elements: R, C, L

Inter-tier coupling



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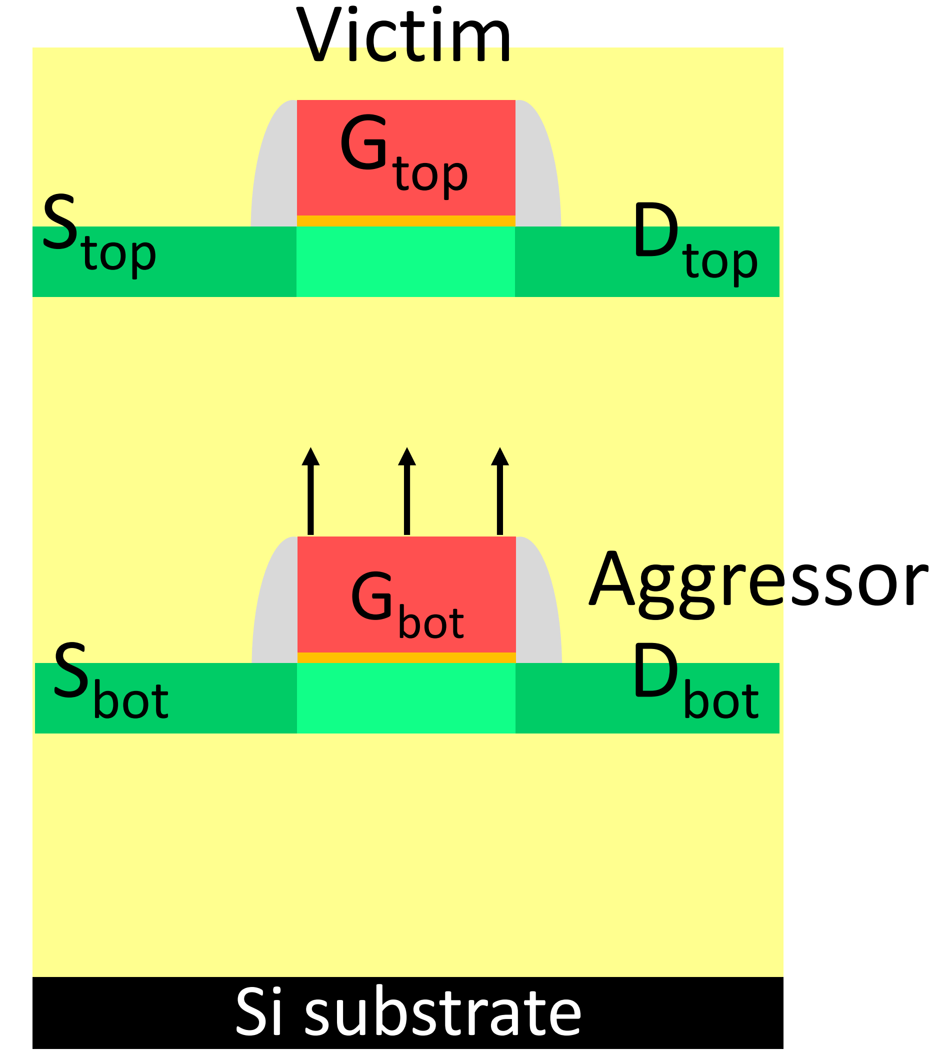

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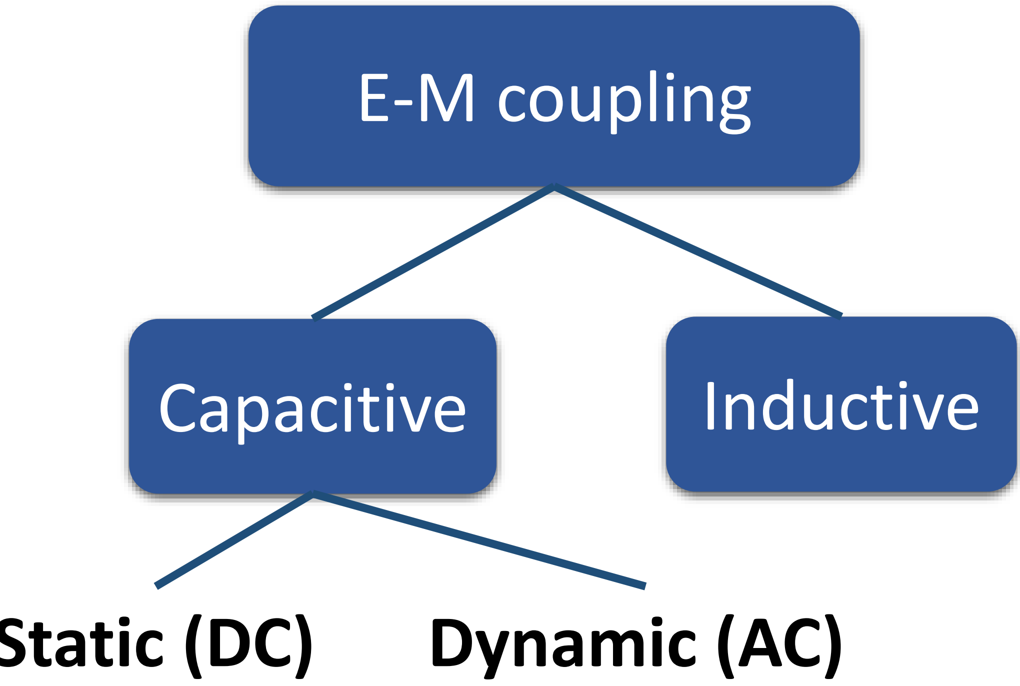

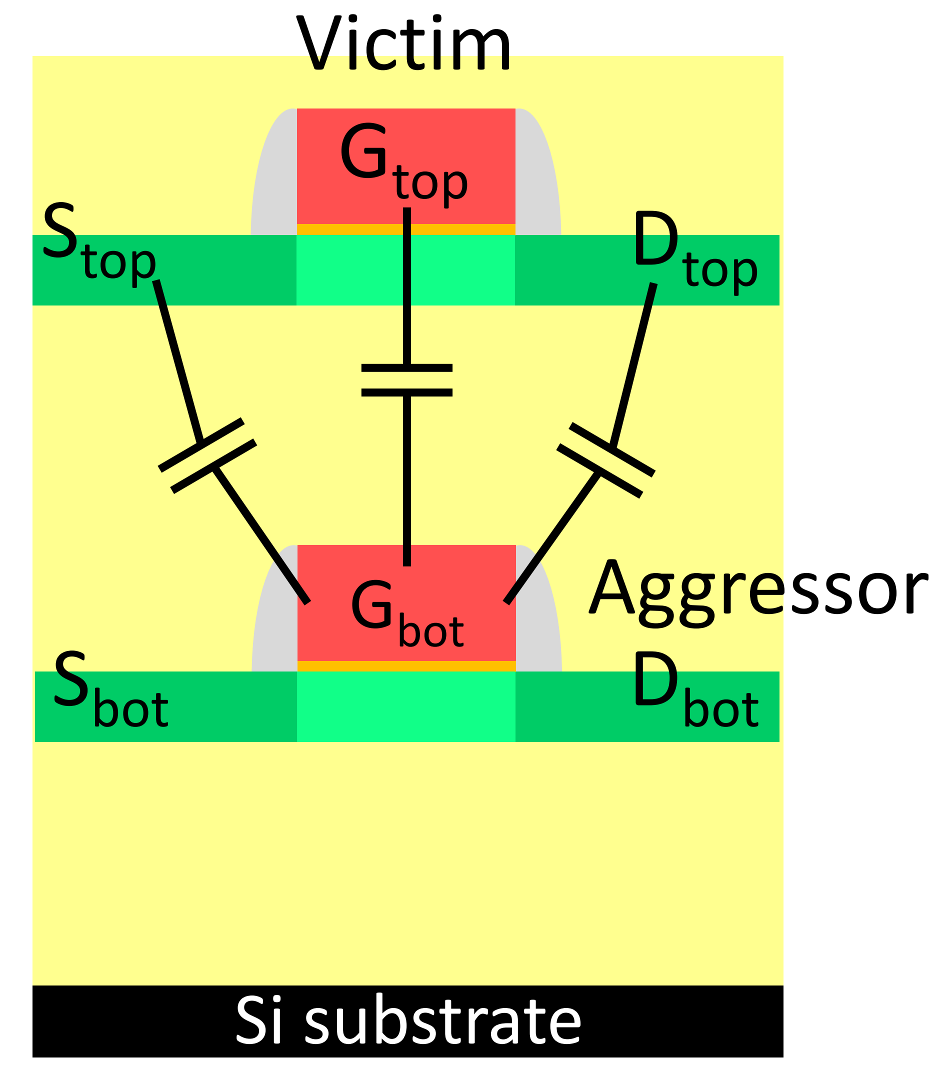

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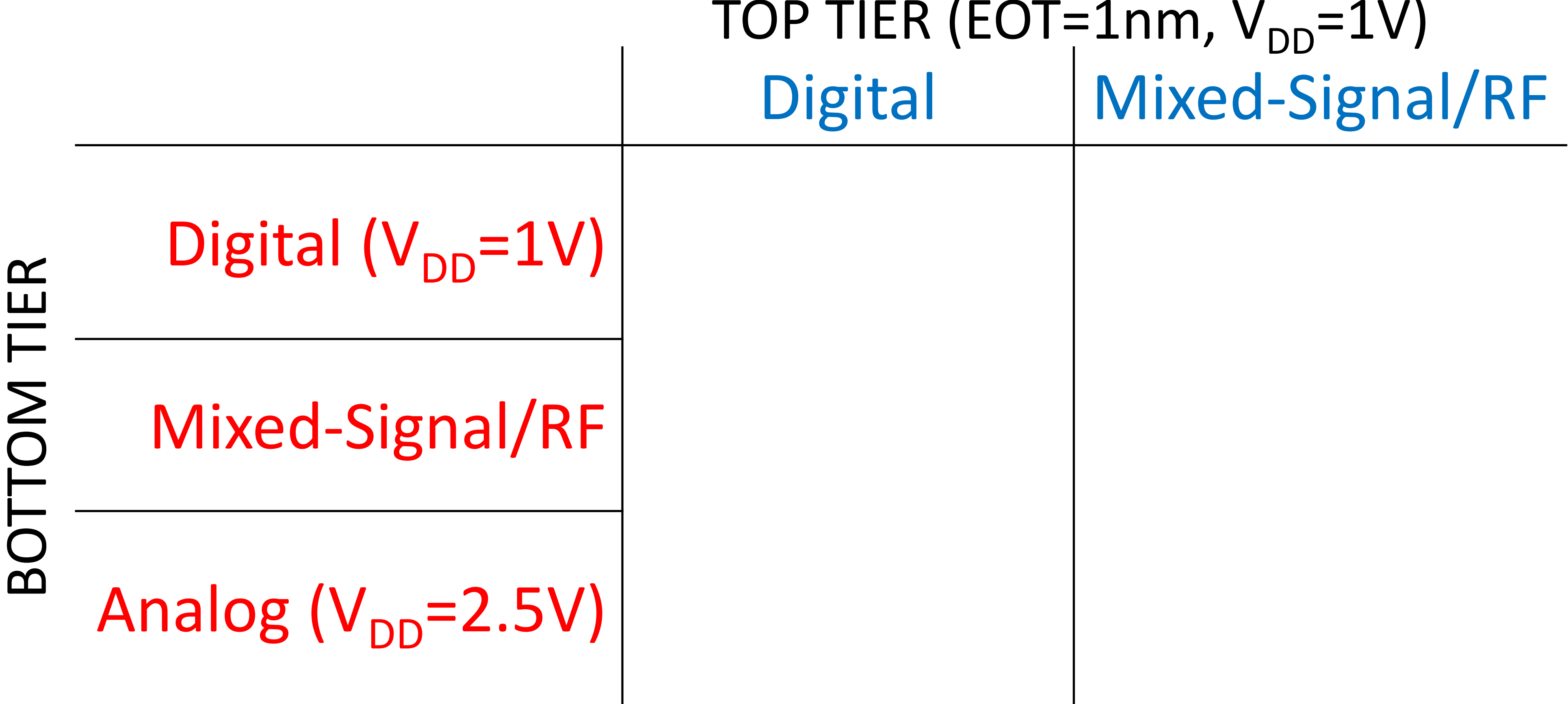
Scope of the study



- Conclude on GP insertion need & investigate GP morphology

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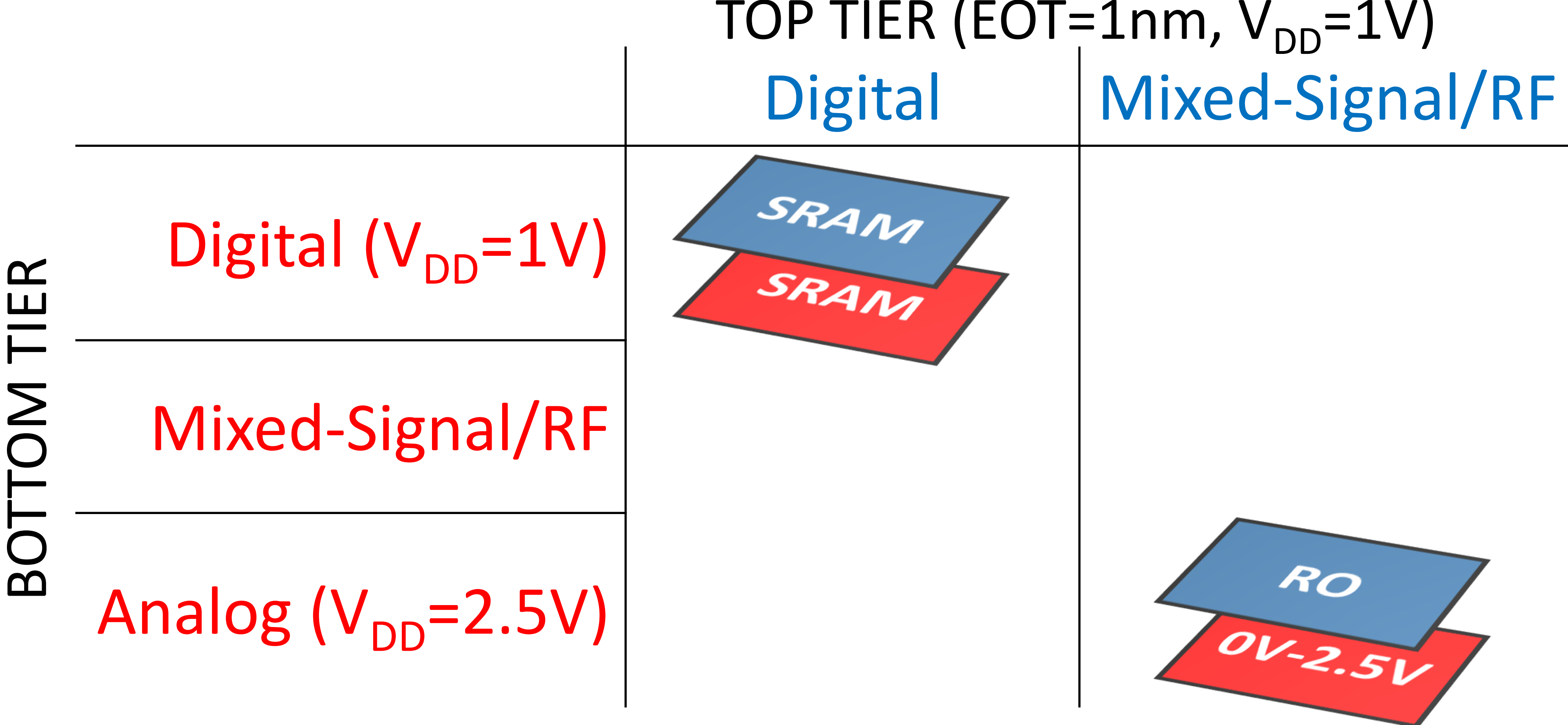

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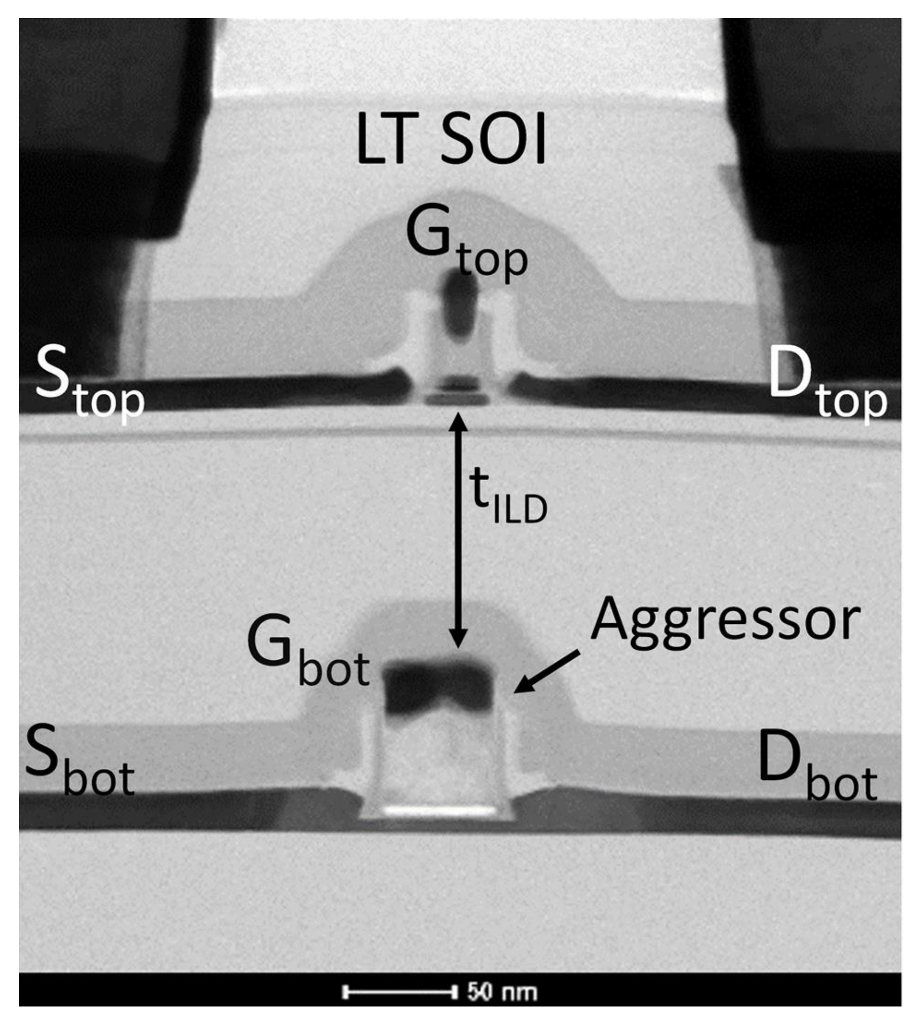
Experimental details

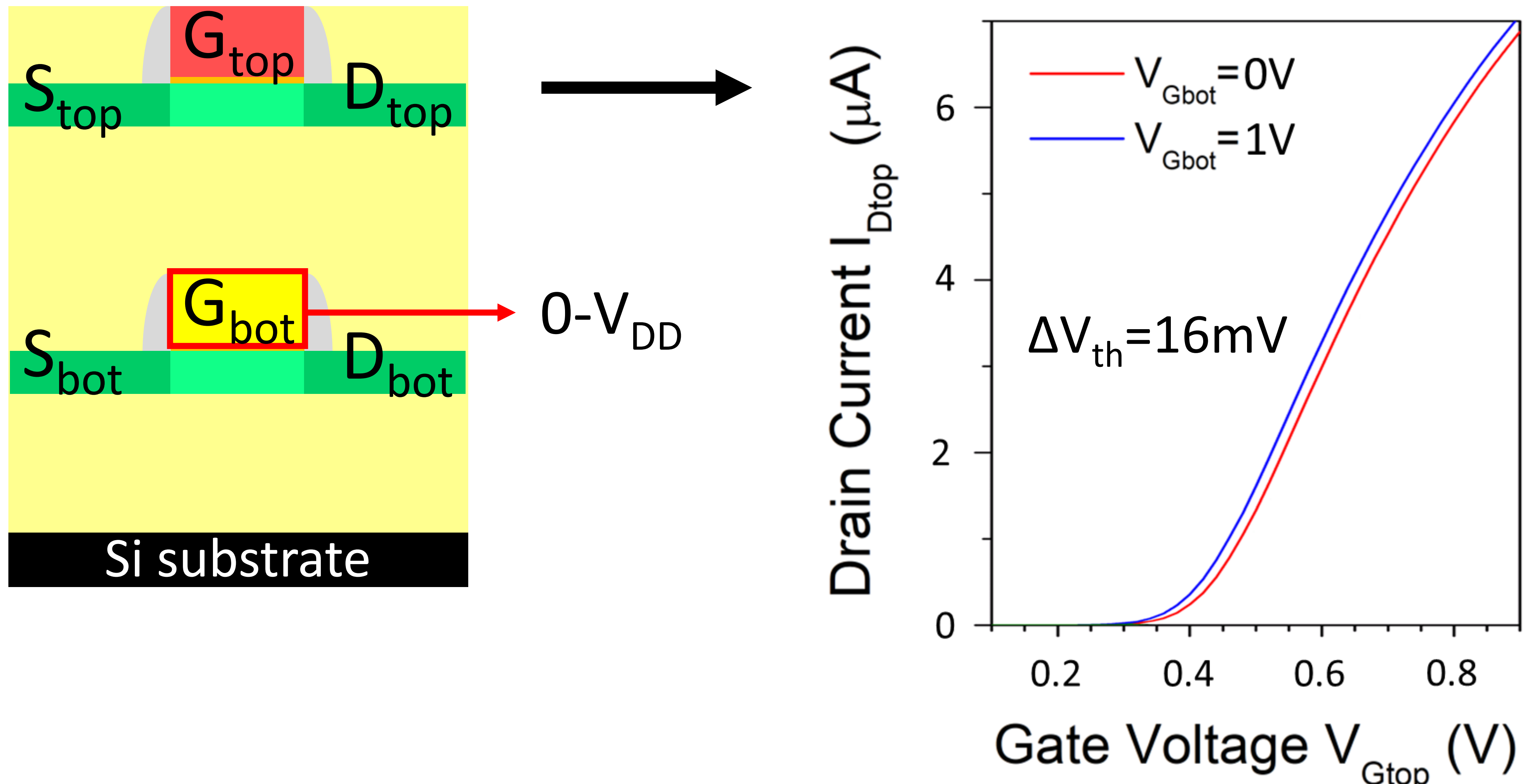


L. Brunet et al., VLSI 2016

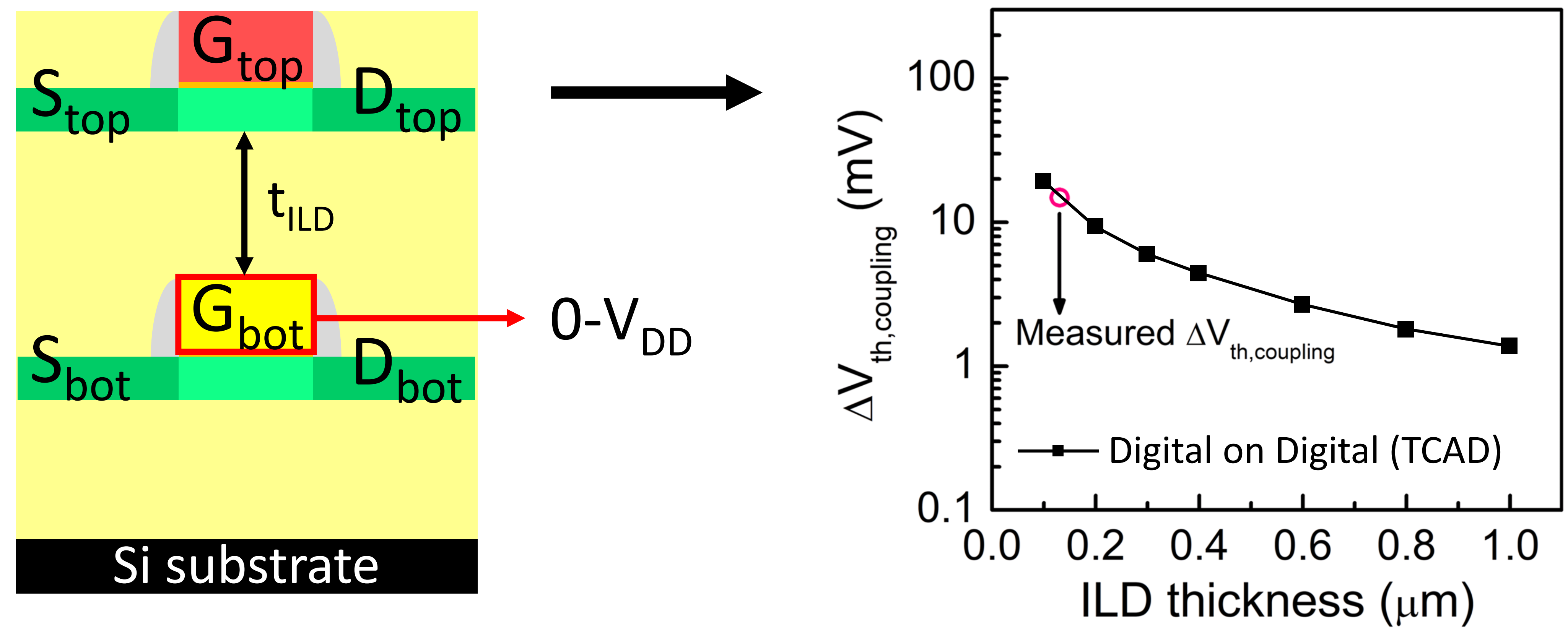
Digital on Digital

- EOT=1nm (V_{DD}=1V)
- t_{si}=7nm
- $L_{G,nominal}$= 28nm
- t_{ILD}=130nm
- No iBEOL
- Limited TB for TOP SOI

Inter-tier Static Capacitive Coupling



Inter-tier coupling vs 28FD local variability



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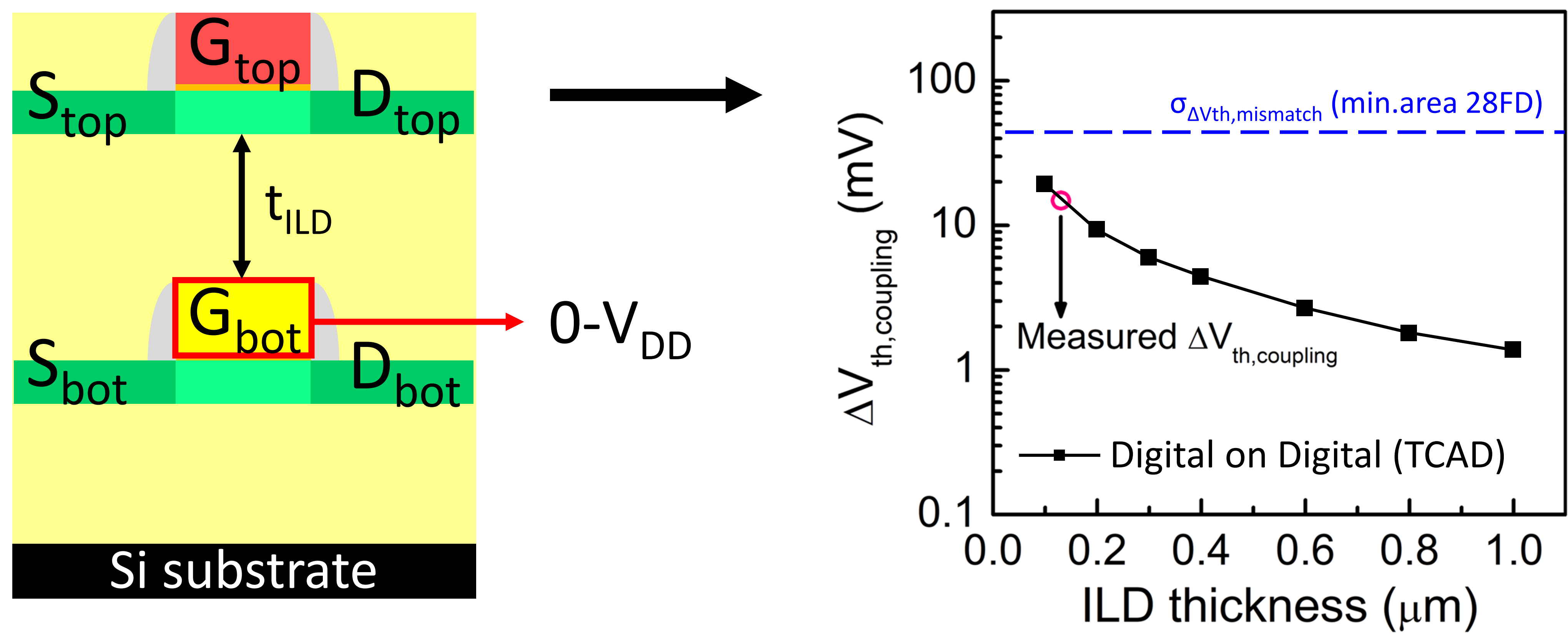

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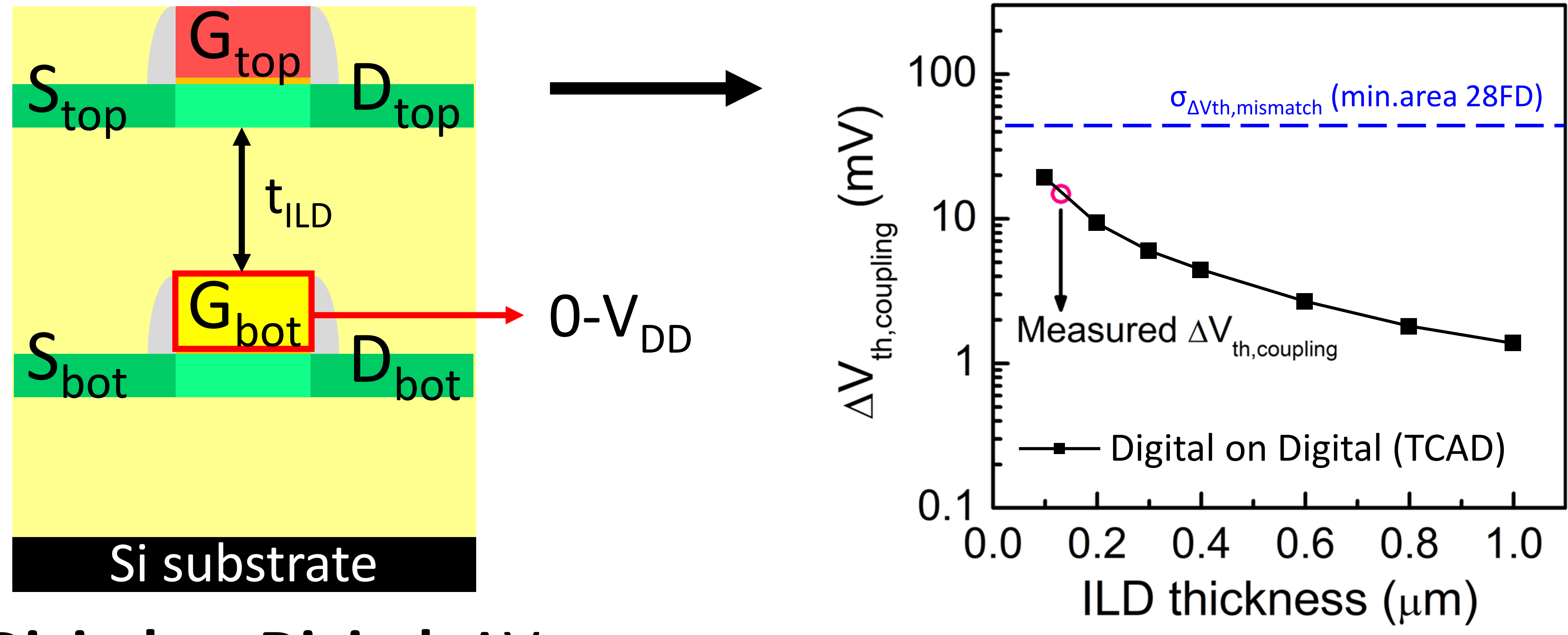

- **Digital on Digital**: $\Delta V_{th,coupl}$ vs $\sigma_{\Delta Vth,mismatch}$
  → Typical range of gate areas is allowed (t_{ILD}=130nm)[1]

[1] P.Sideris et al., EUROSOI 2019

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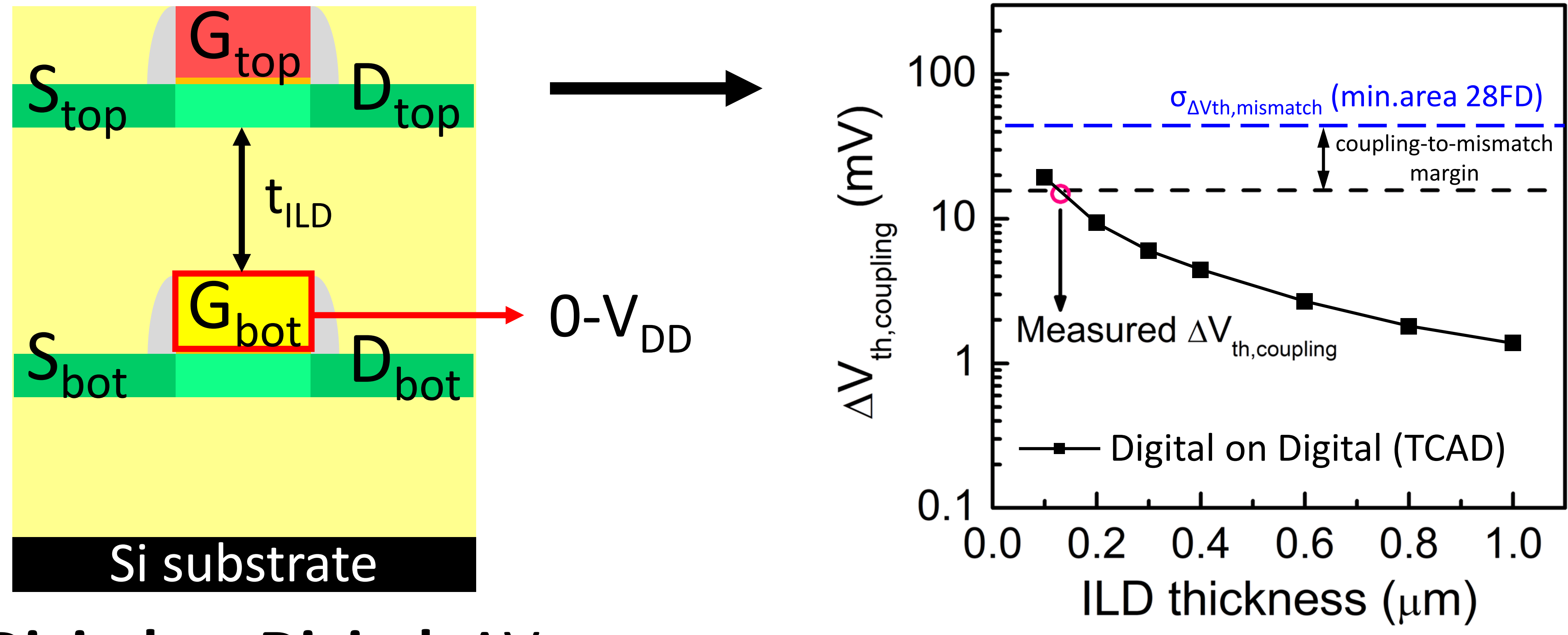

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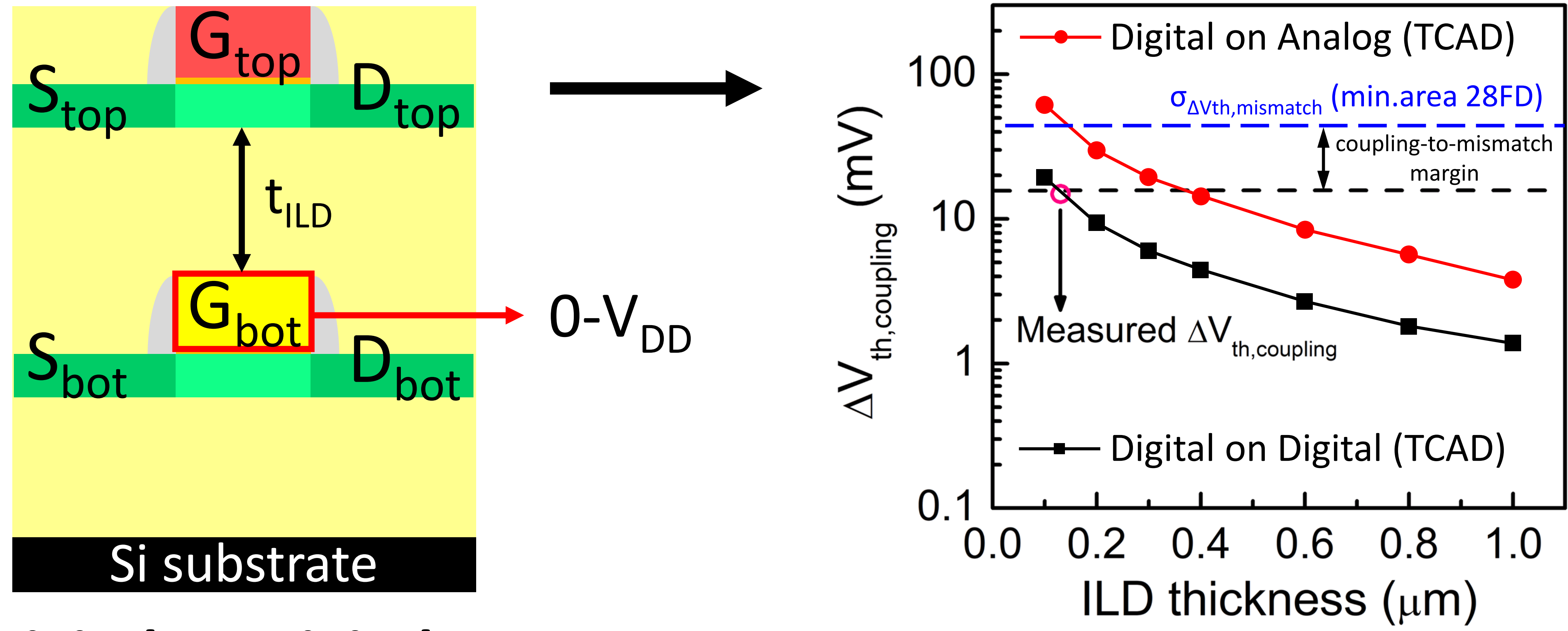

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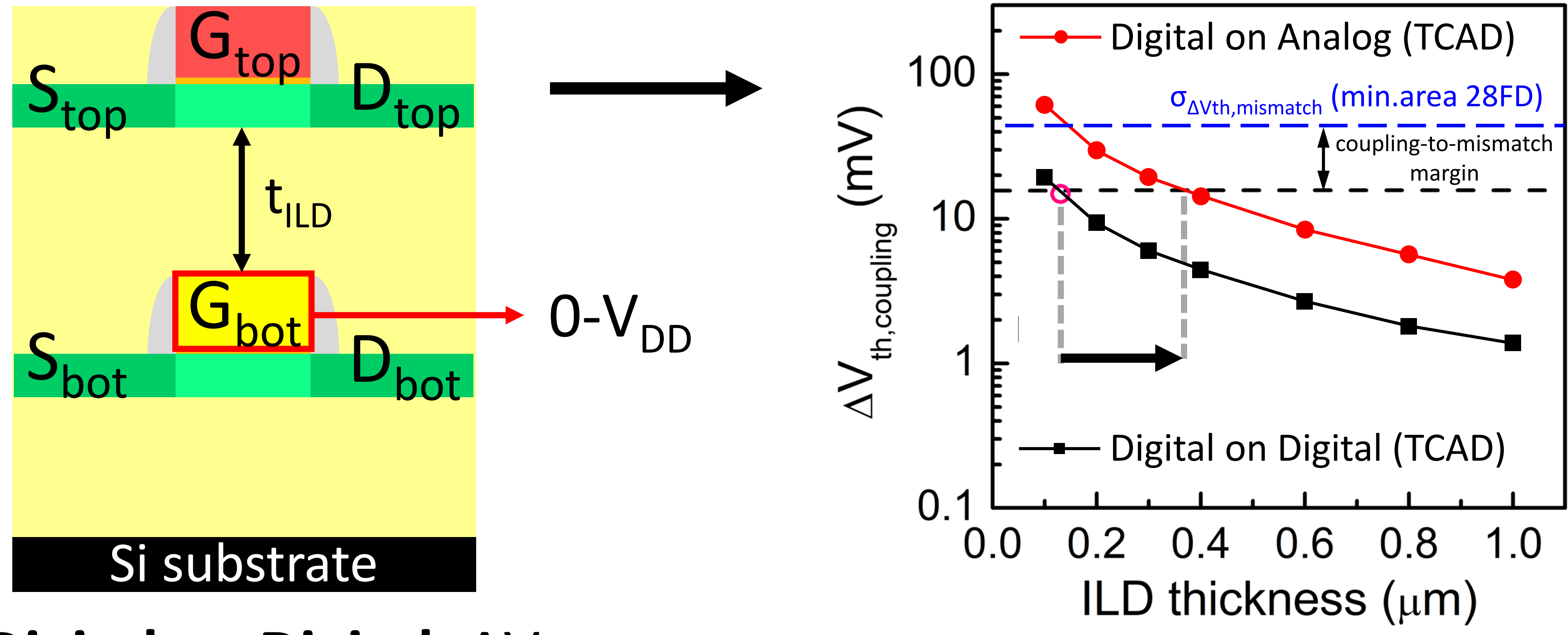

- **Digital on Digital**: $\Delta V_{th,coupl}$ vs $\sigma_{\Delta Vth,mismatch}$
  → Typical range of gate areas is allowed (t_{ILD}=130nm)[1]
- **Digital on Analog**: t_{ILD}≥350nm or GP insertion

[1] P.Sideris et al., EUROSOI 2019

Impact of gate length

- $\Delta V_{th,coupl}$ decreases for smaller L_G

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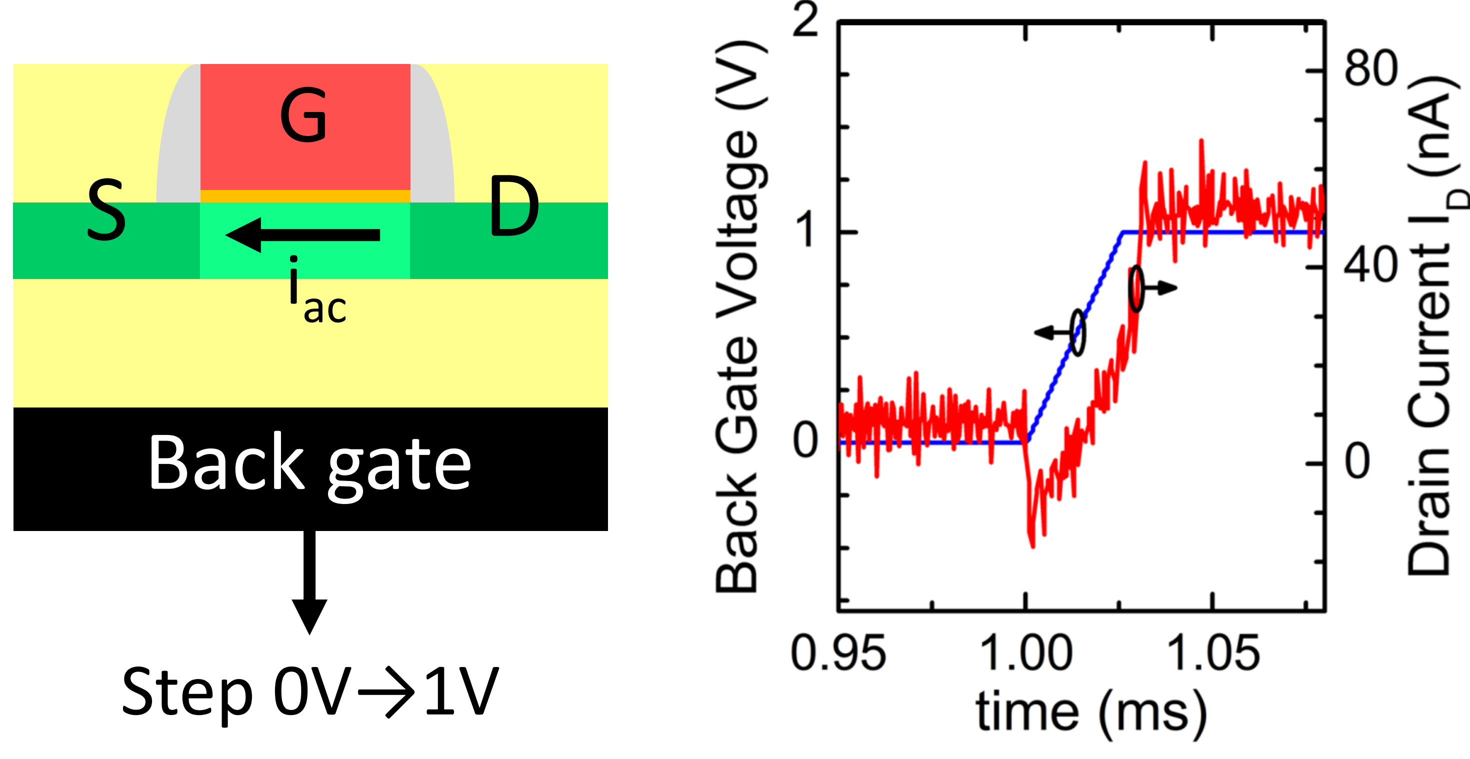
- 28FD nominal L_G top devices show better immunity

Inter-tier Dynamic Capacitive Coupling



- Fast switching of BG, can result in parasitic spikes ($i_{ac,coupl}$) at I_{dtop}

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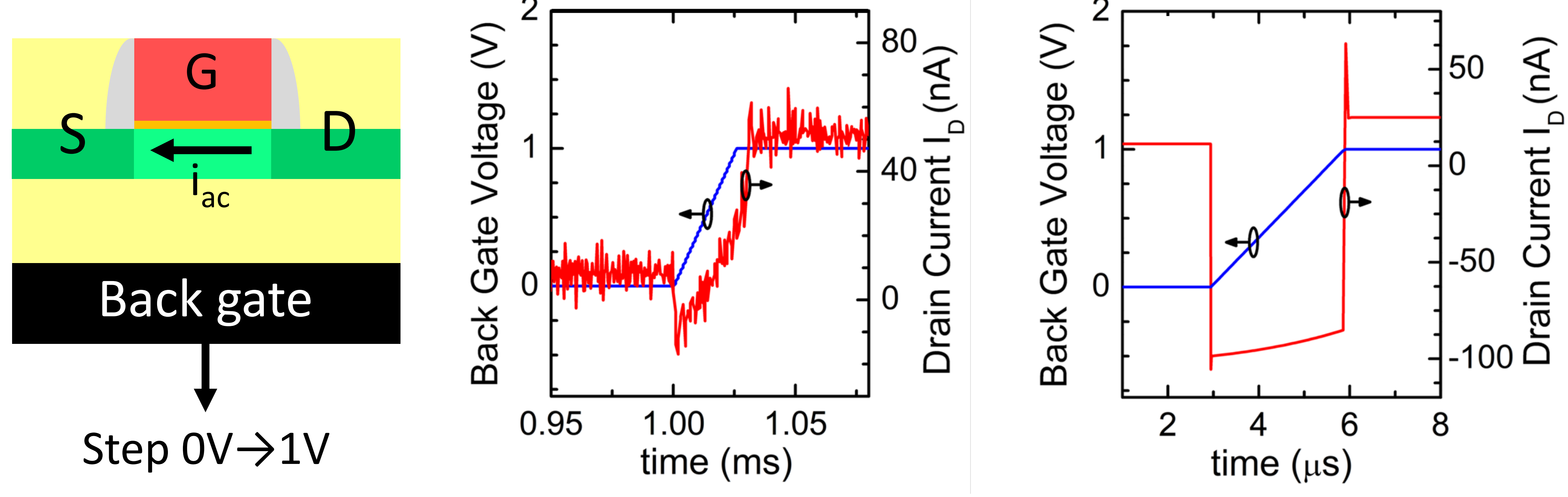

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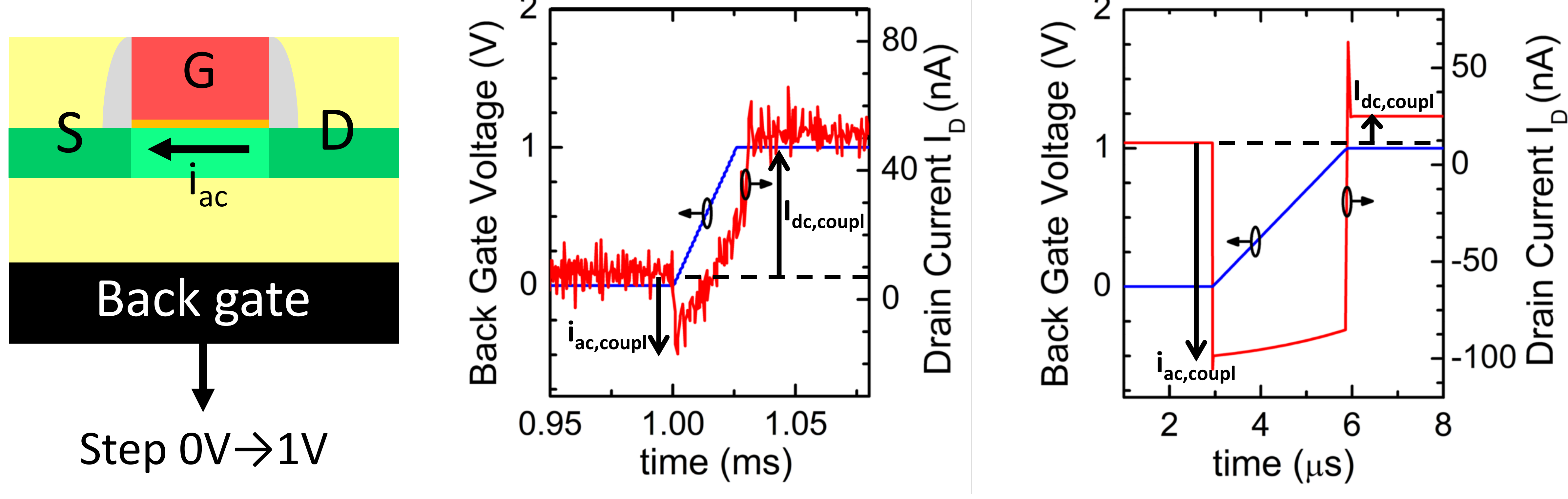
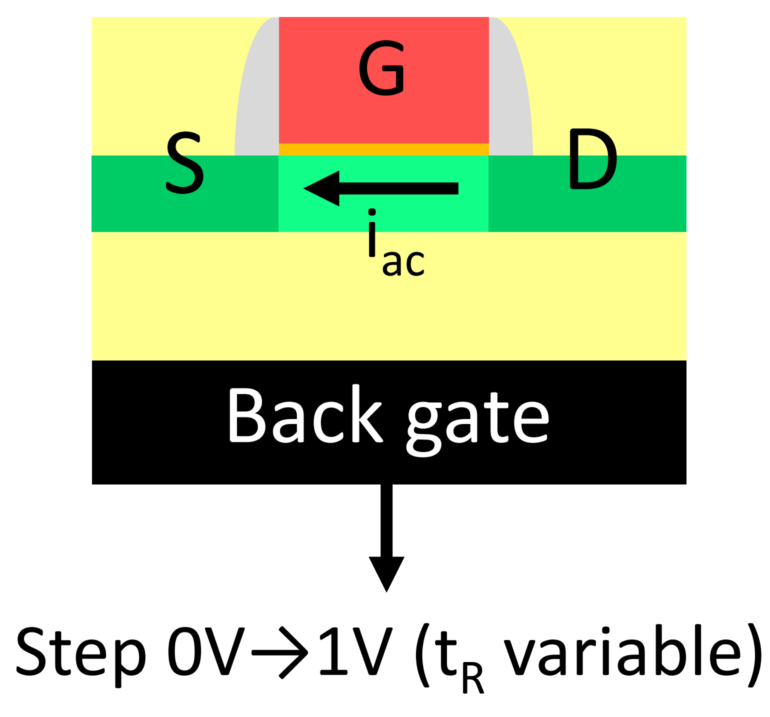
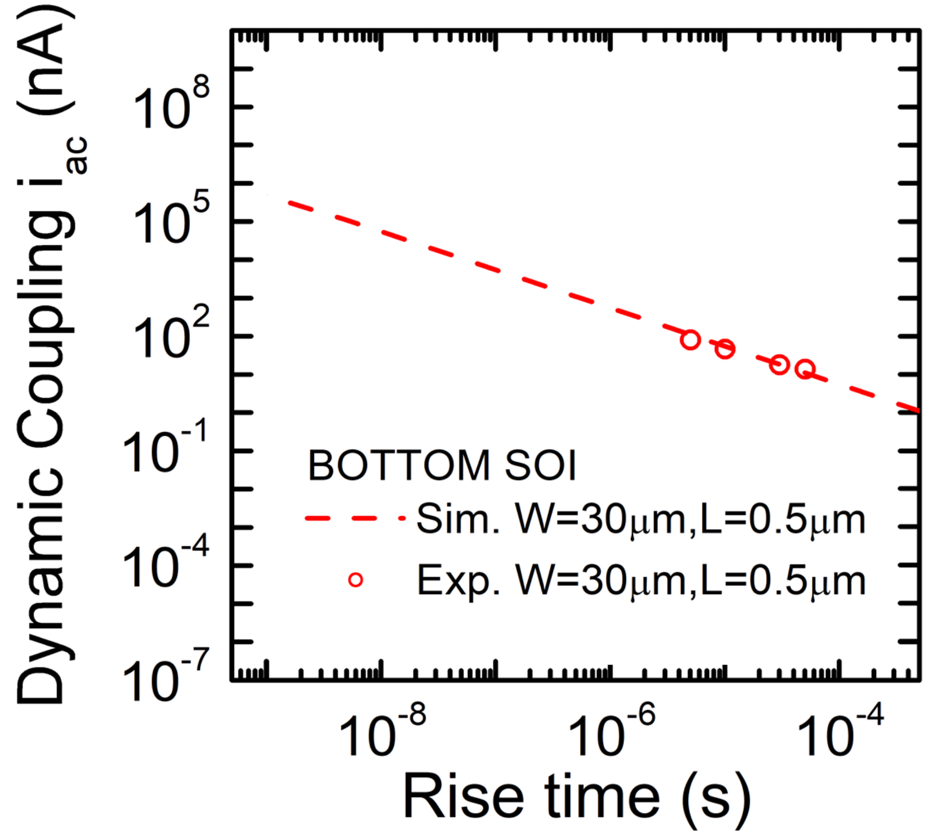


- Fast switching of BG, can result in parasitic spikes ($i_{ac,coupl}$) at I_{dtop}
- Shorter t_R of V_{Gbot}, increased $i_{ac,coupl}$ → AC more critical than DC coupling

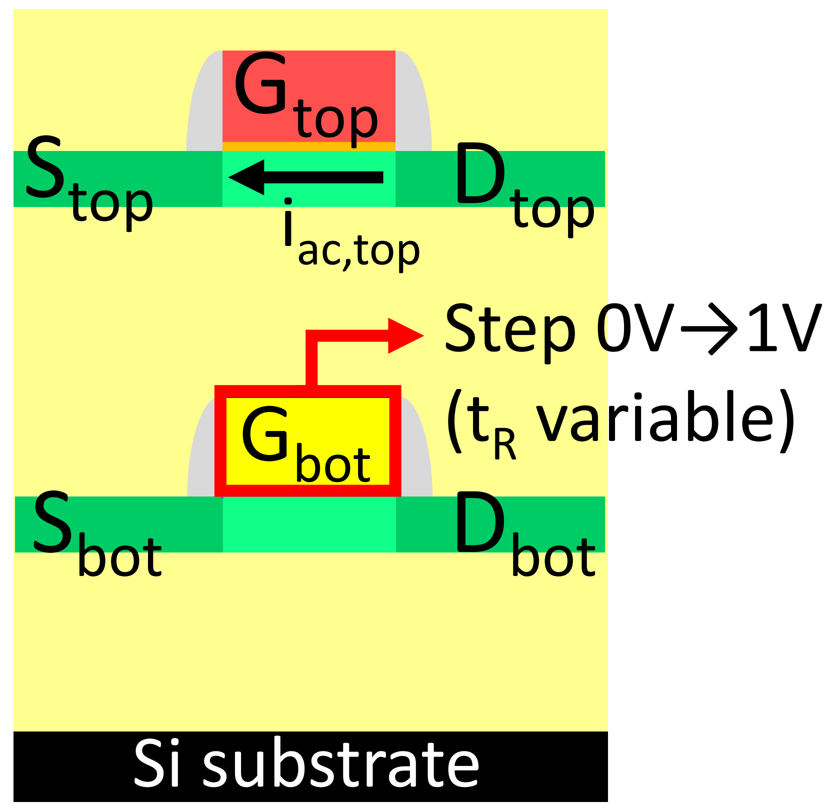
Impact of switching time

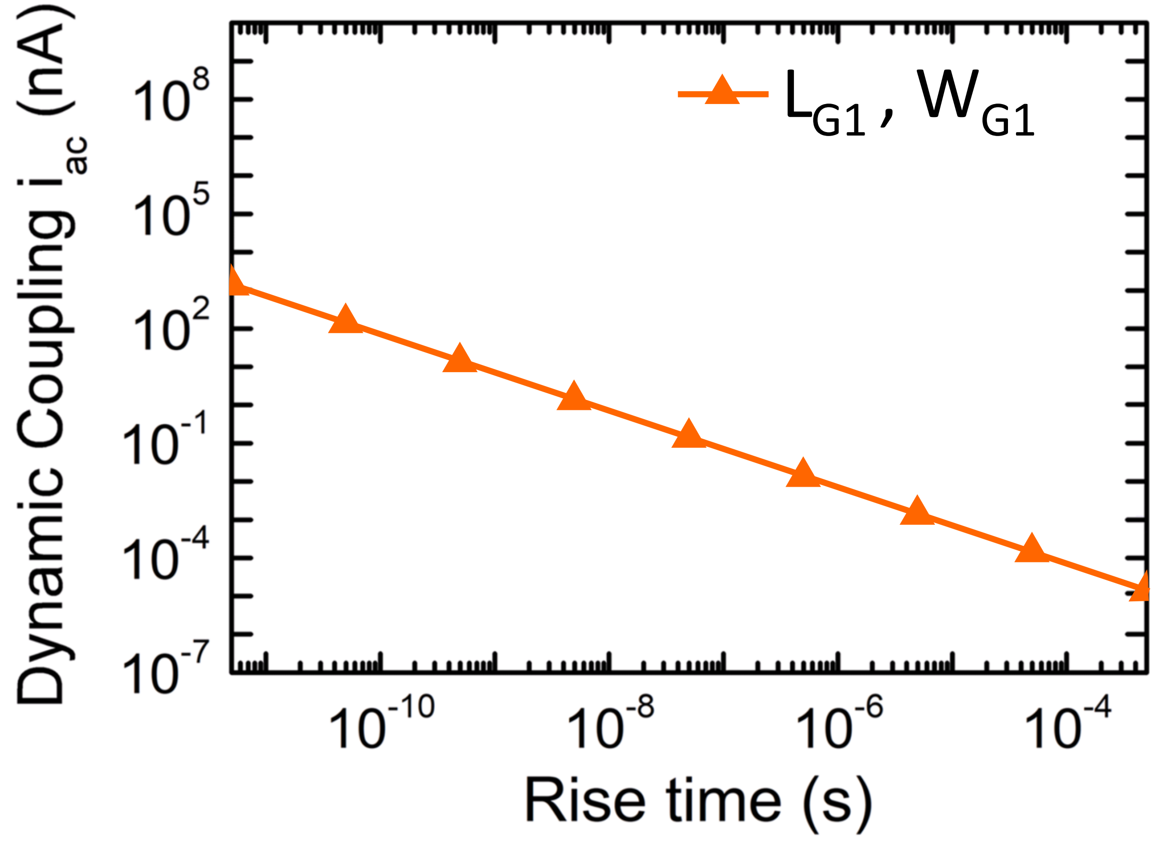




- TCAD vs experimental: consistent results
- Extrapolation for shorter rise times: dependence on Ohm's law

Impact of gate length & width





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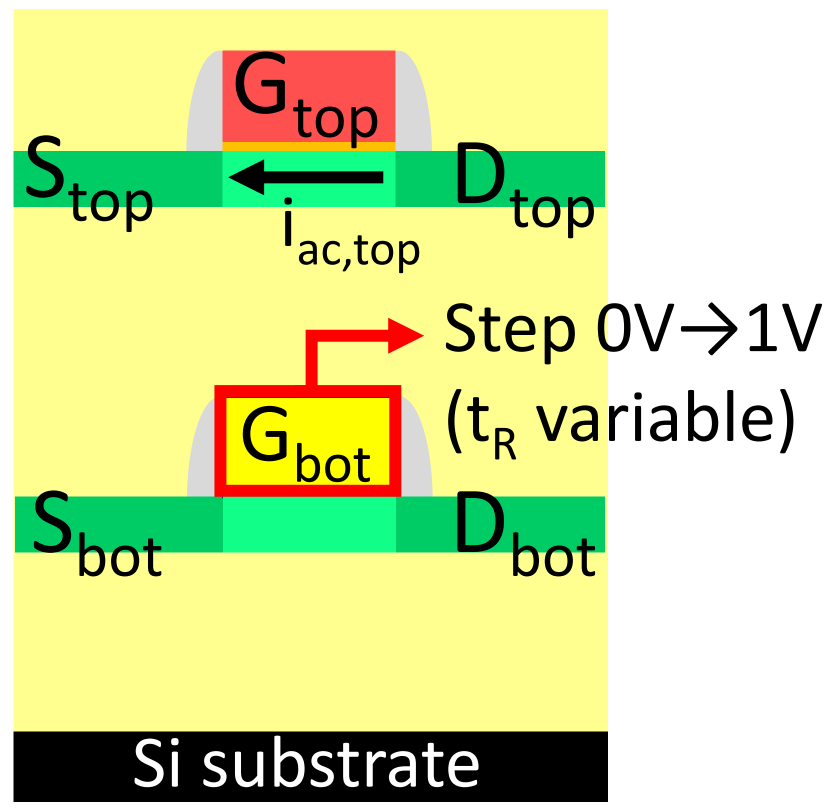

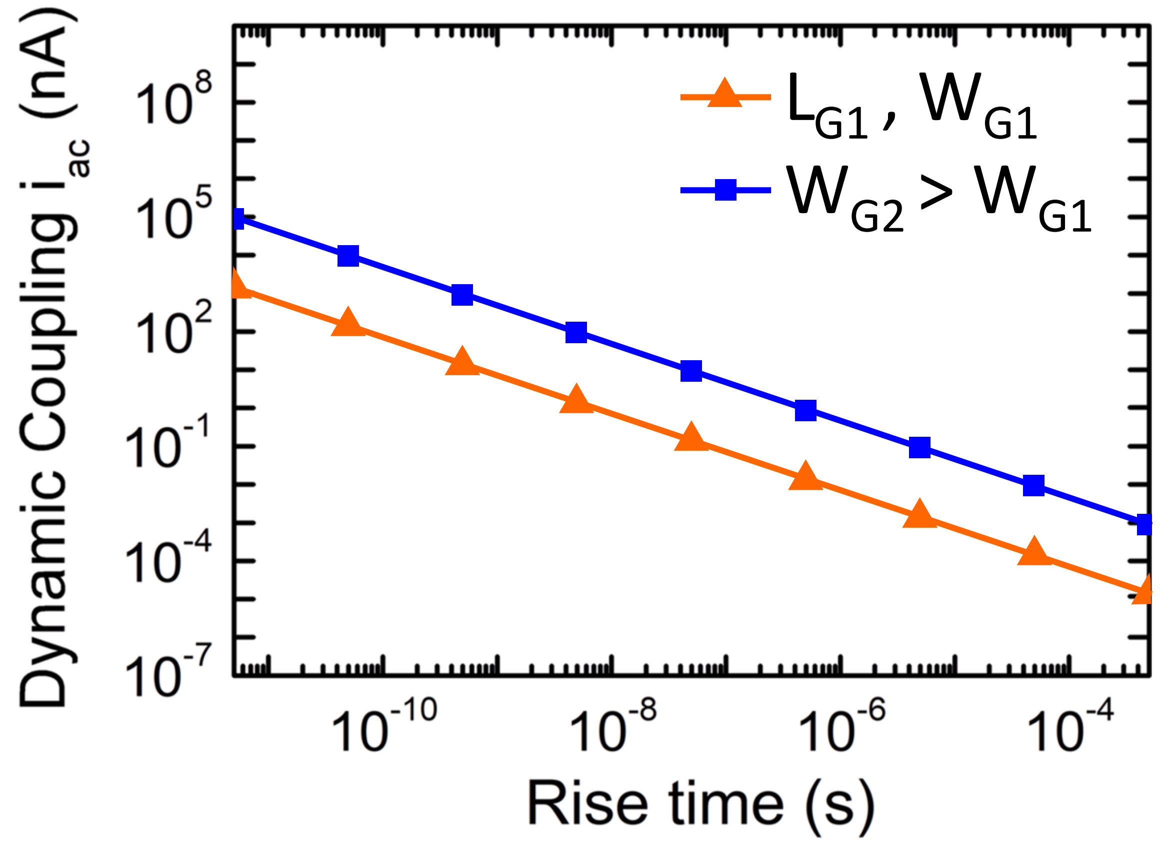

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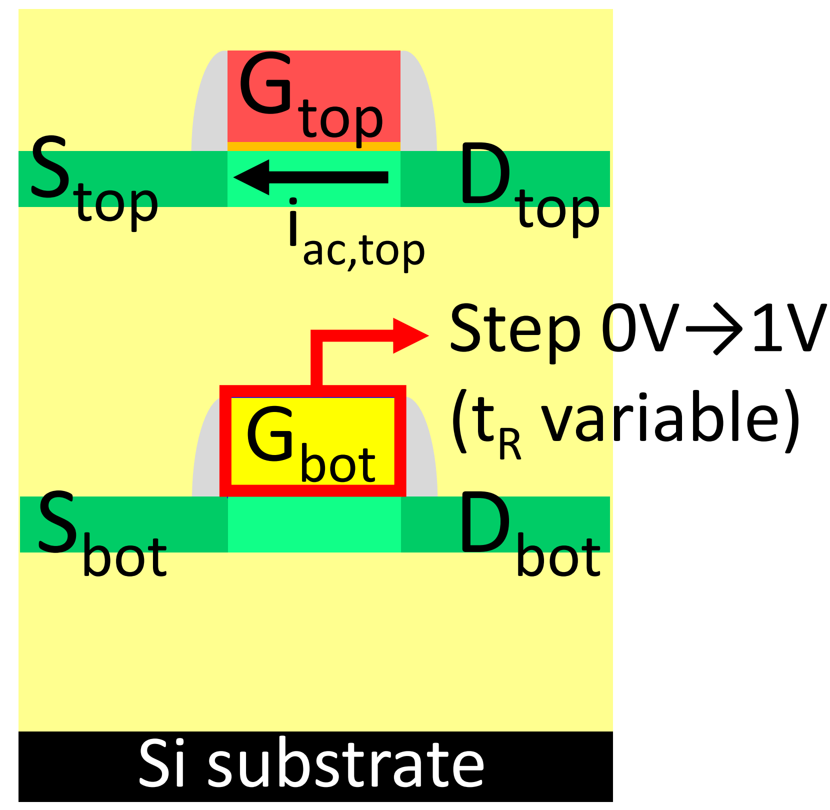

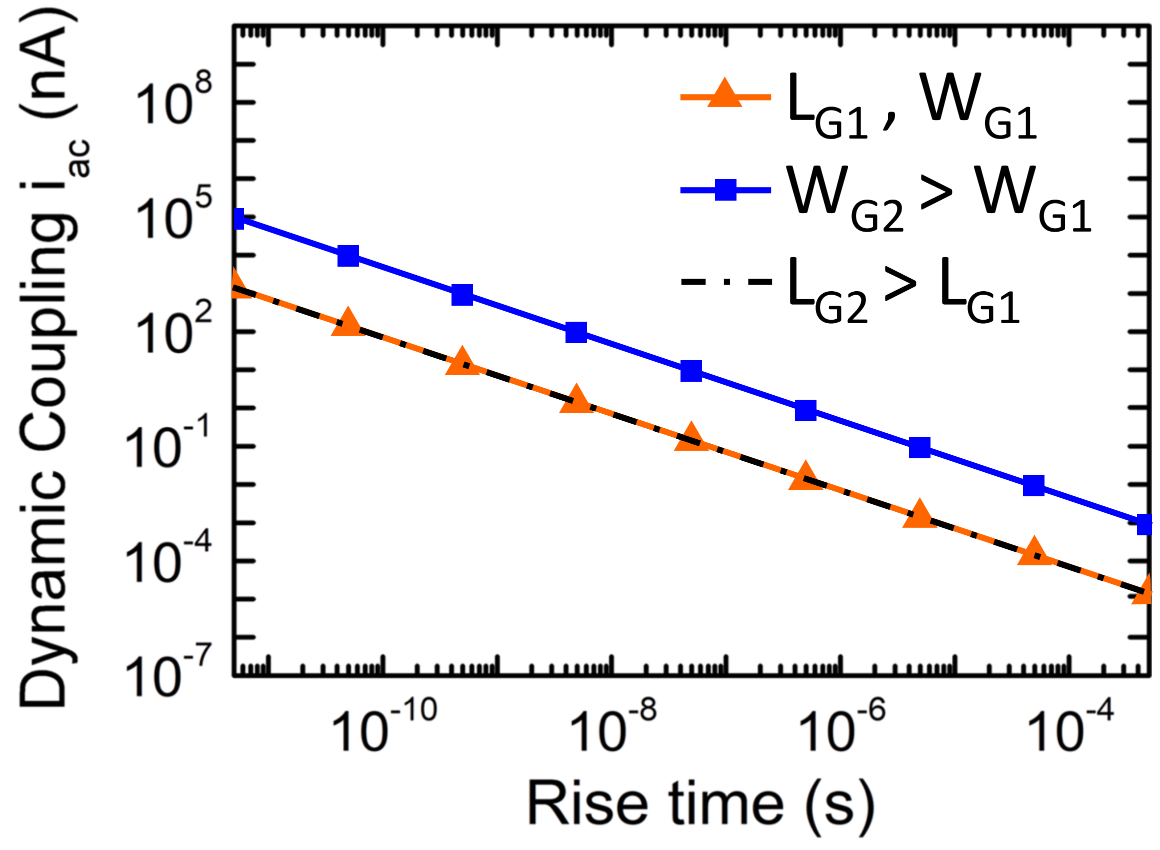

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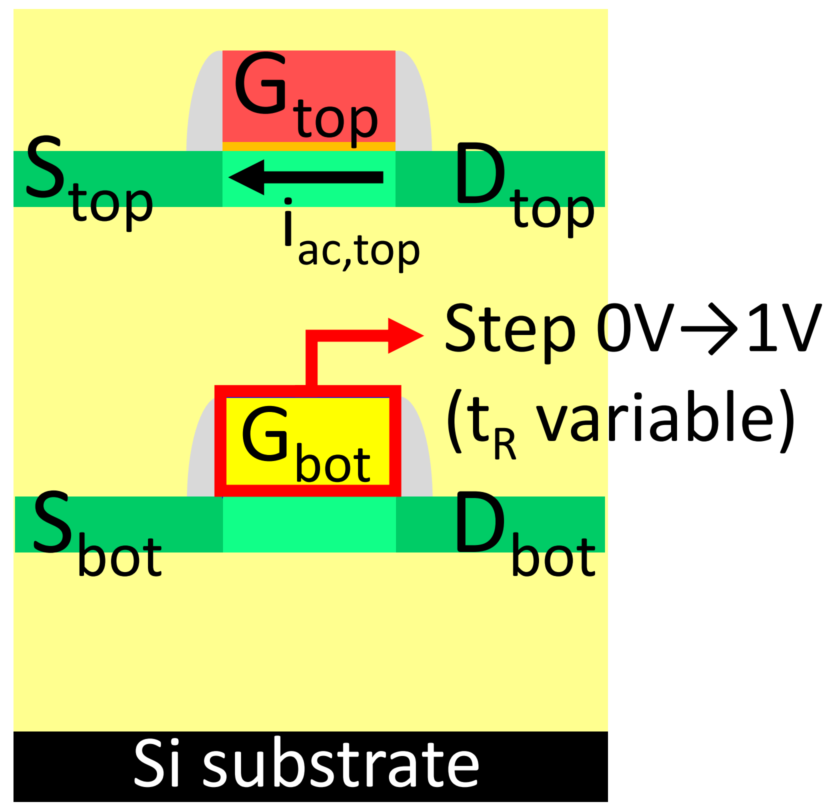
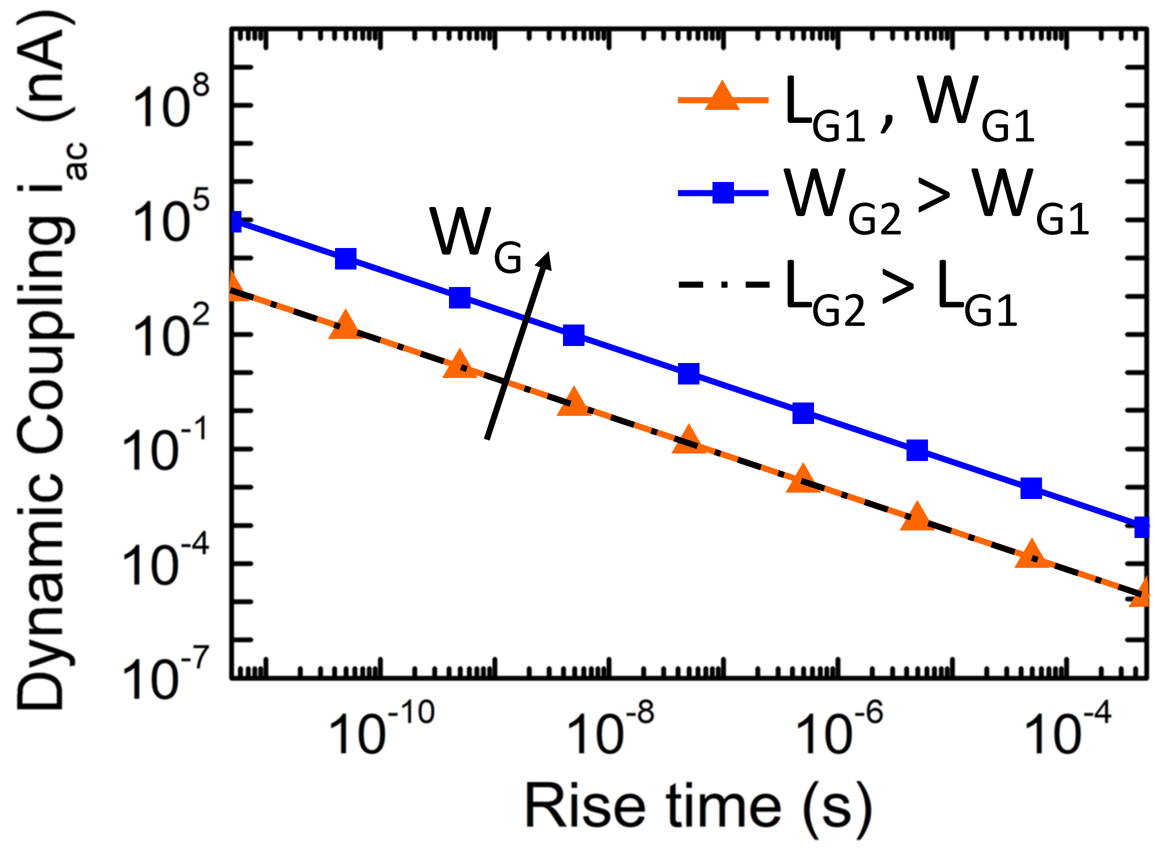
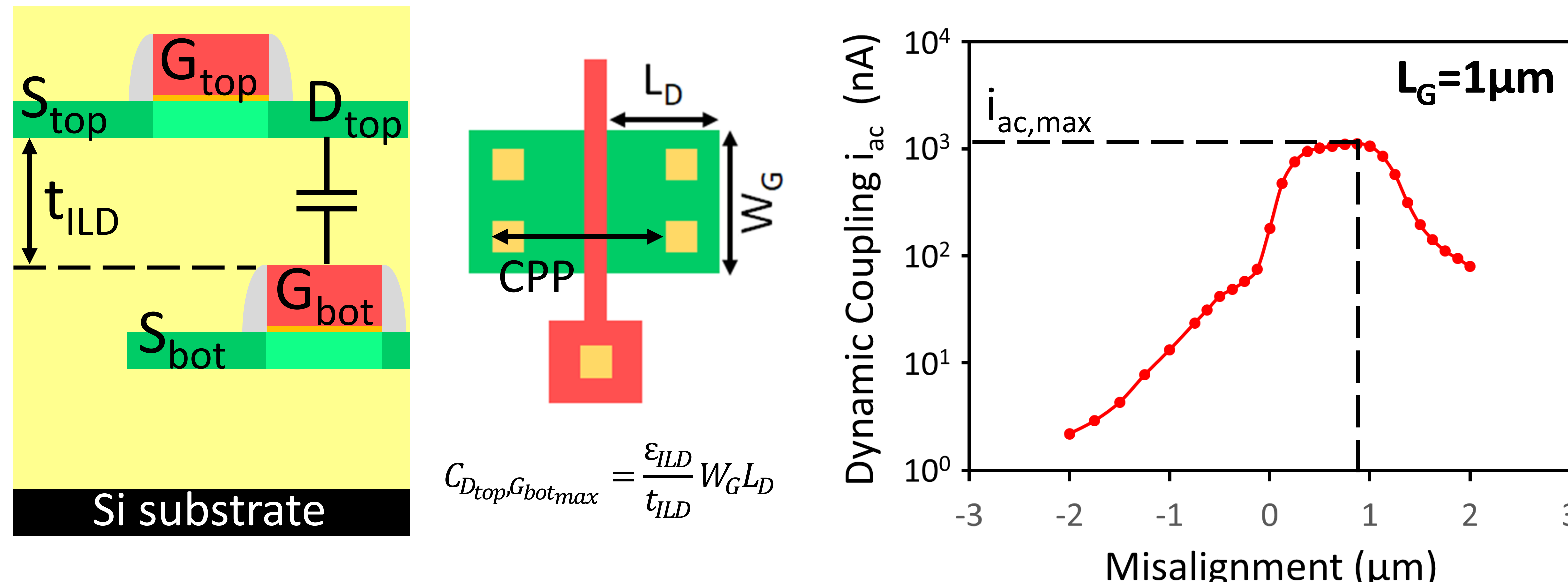




- Dynamic coupling dependent on W_G but not on L_G

Impact of top-bottom misalignment



- $C_{Dtop,Gbot}$ critical → Maximum when D_{top}, G_{bot} overlap

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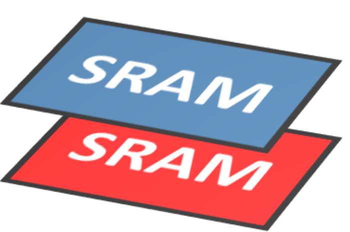
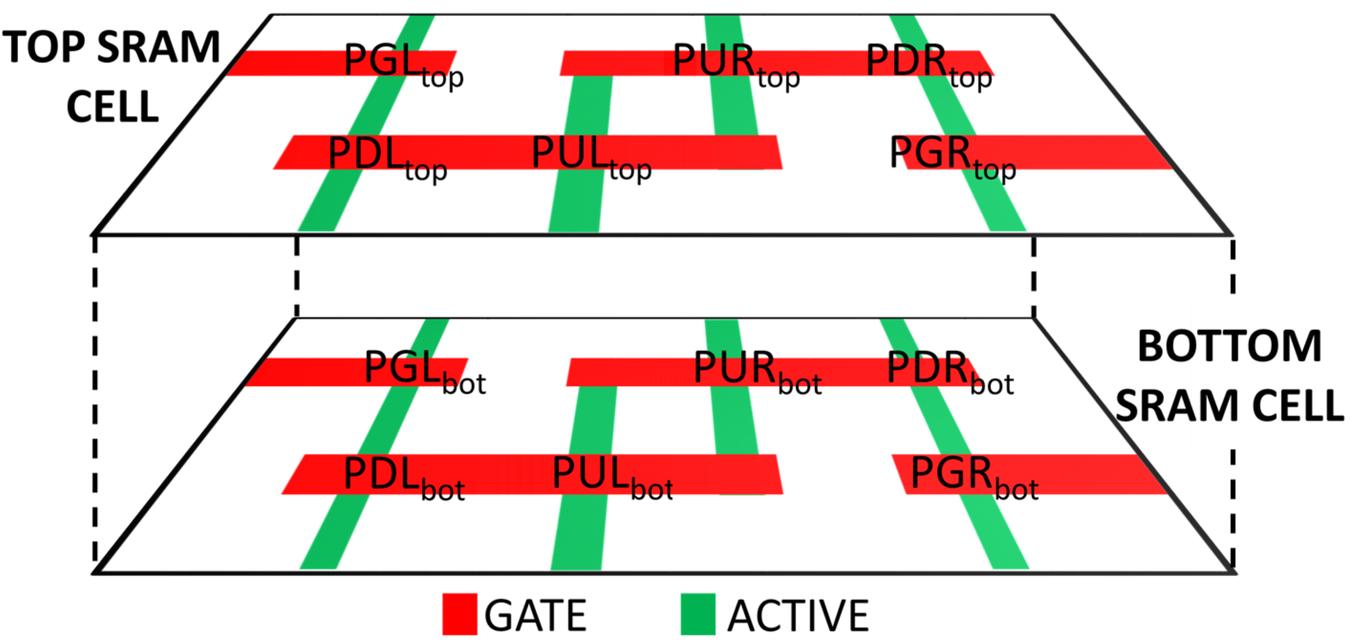
2-bitcell S3D SRAM





Identical 6T-SRAM cells stacked – Aligned with 0 & 100% offset

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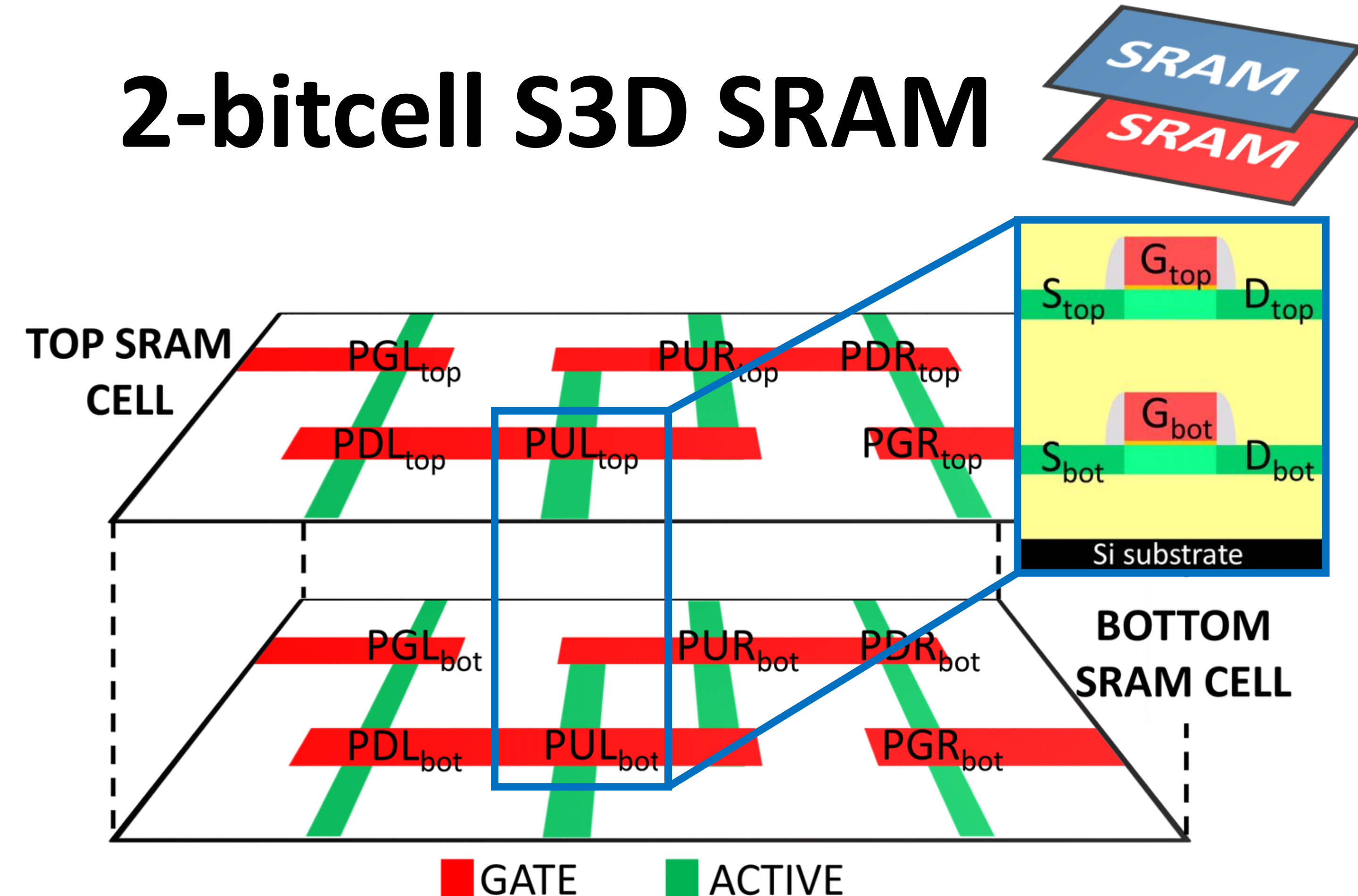

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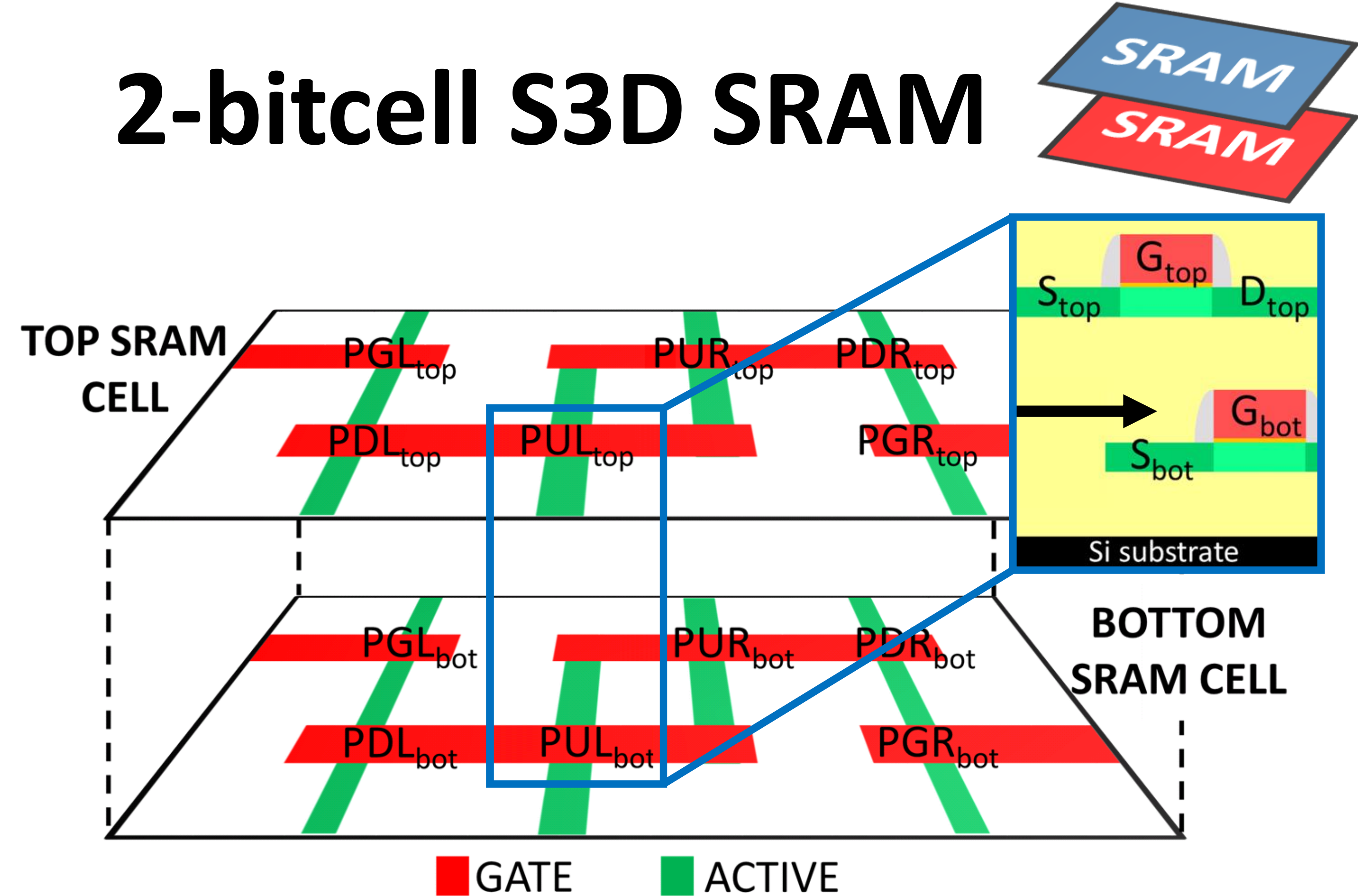

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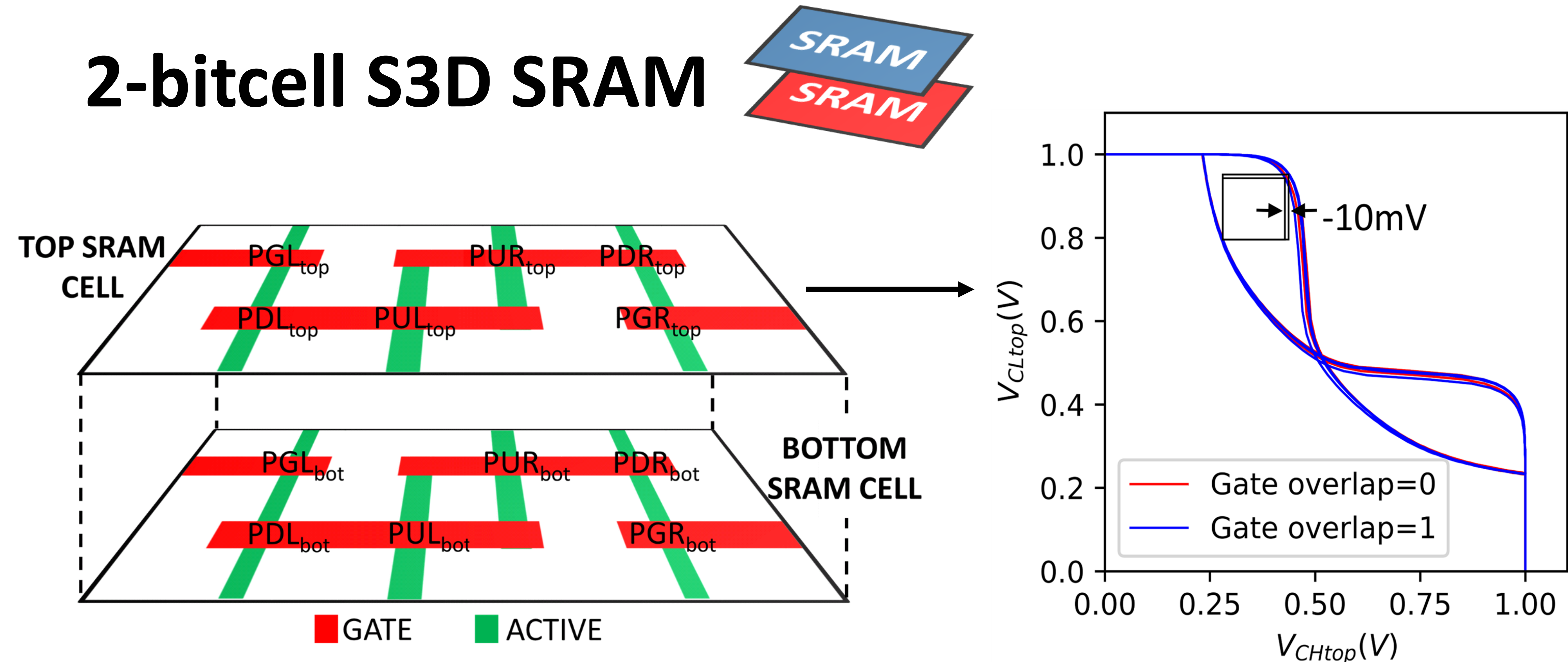
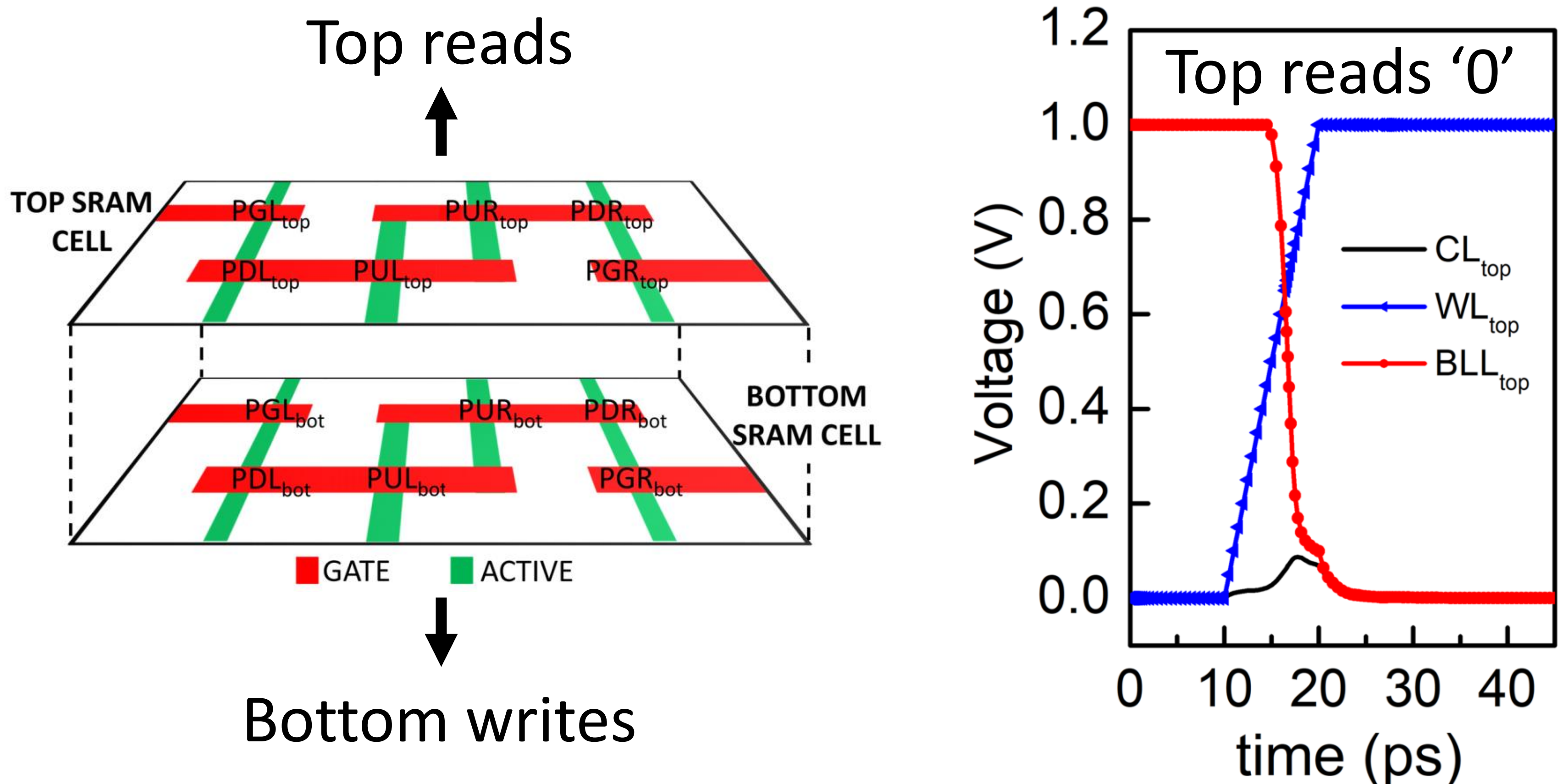


Identical 6T-SRAM cells stacked – Aligned with 0 & 100% offset

- Negligible reduction of SNM[1]

[1] P.Sideris et al., Solid-State Electronics, 2019

Dynamic coupling impact on Read-operation



<u>Top-SRAM read-attempt while bottom-SRAM writes</u>

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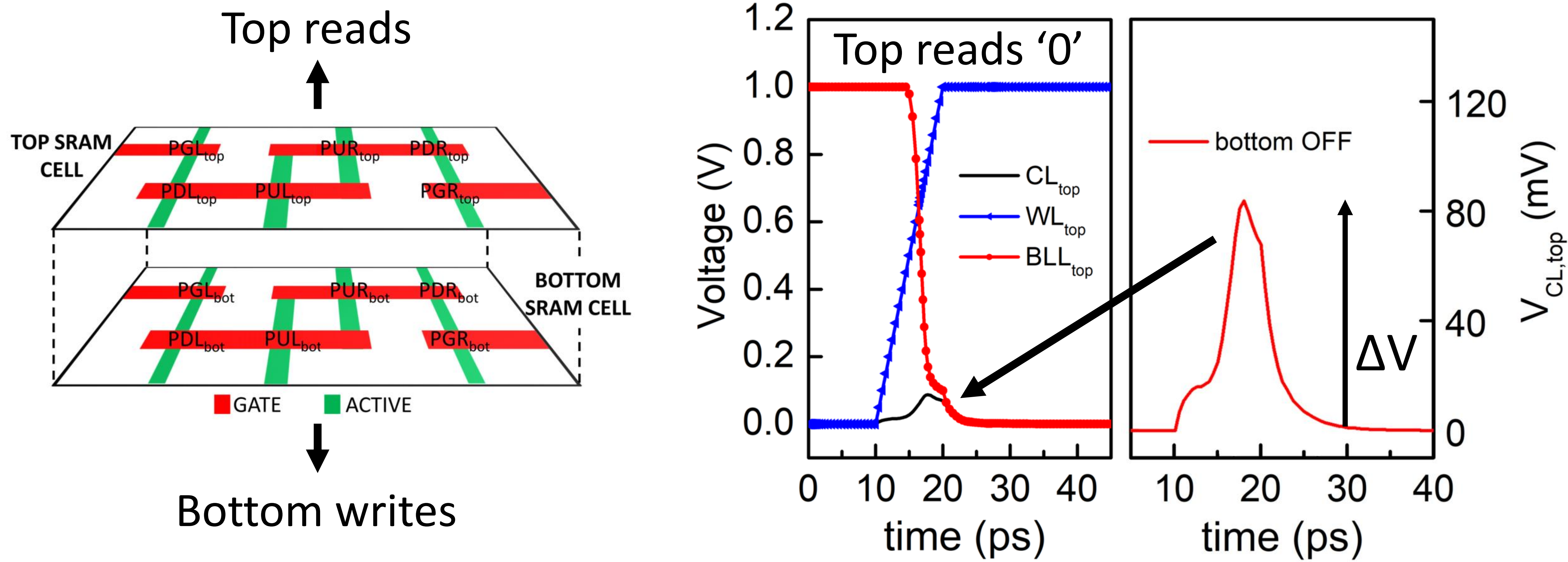

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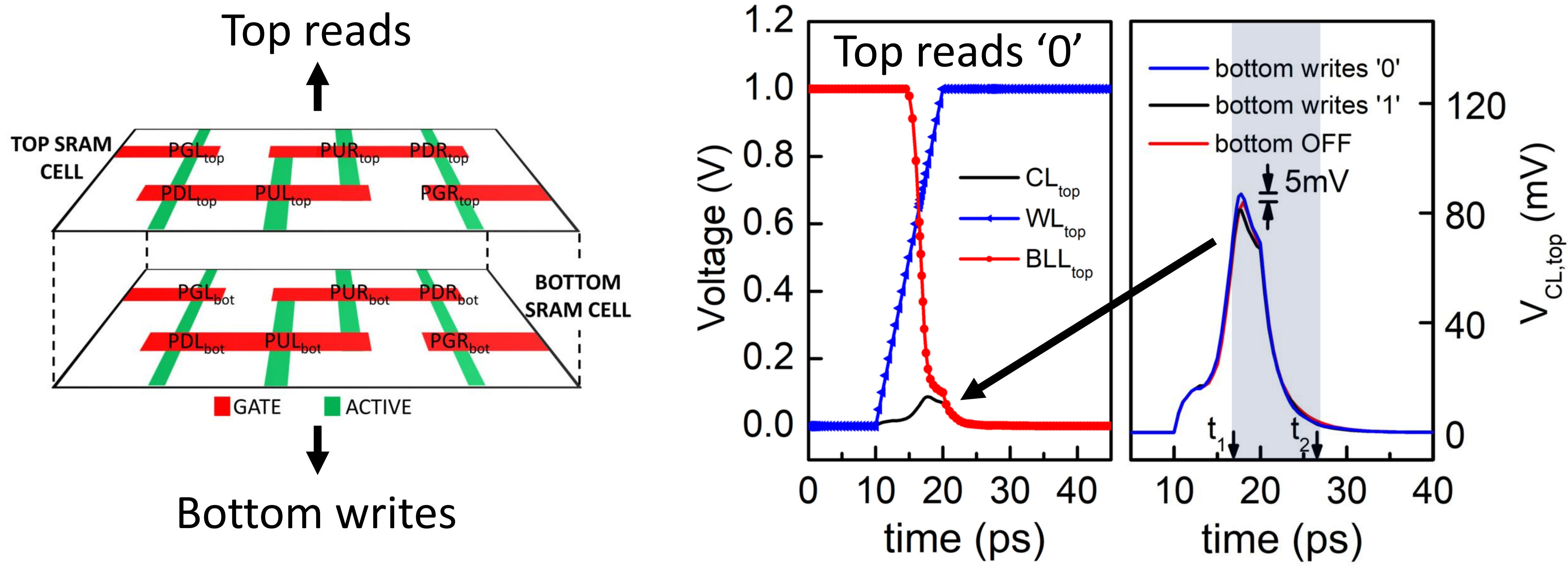

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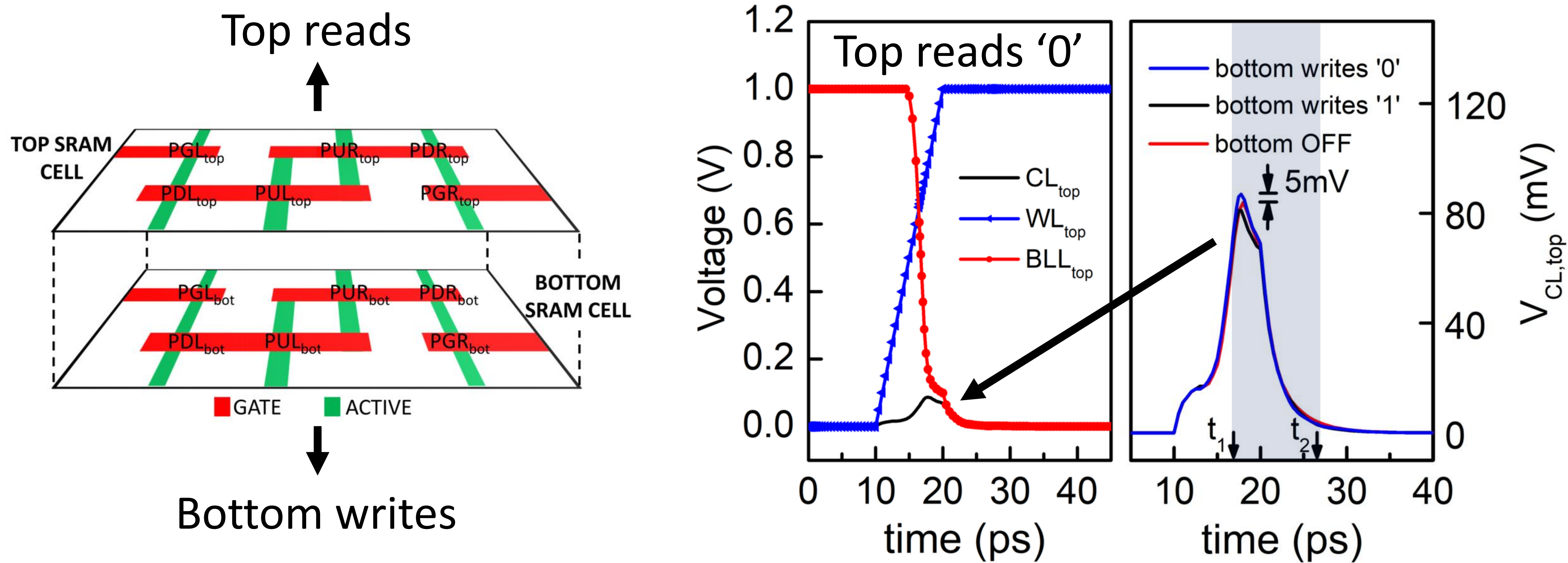
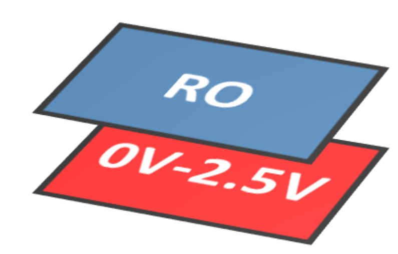
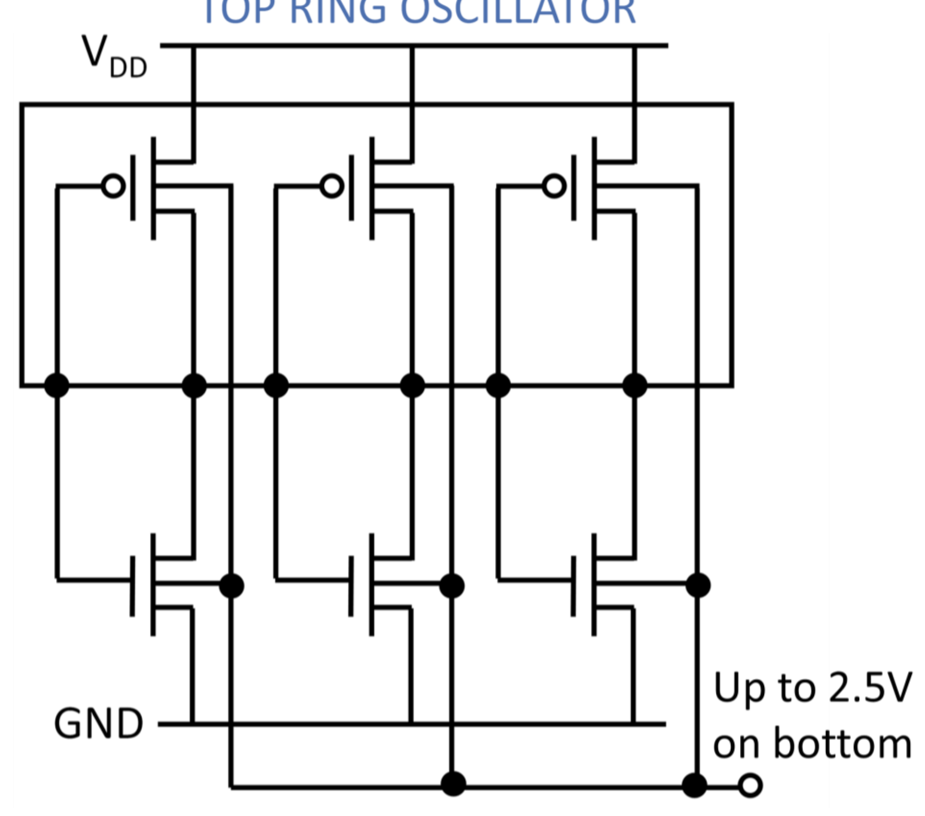


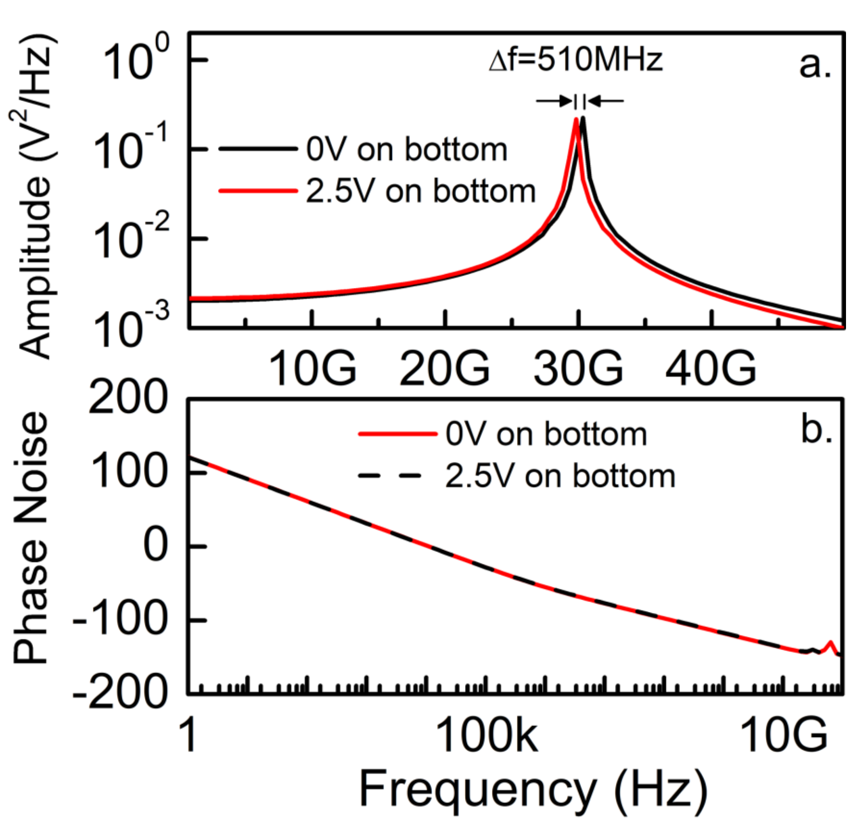
Top-SRAM read-attempt while bottom-SRAM writes

- Negligible impact for shortest rt in 28FD – **No GP needed**

RO stacked on Analog layer







- Top RO output frequency sensitive to V_{Gbot} – **Need for GP**
- No impact on RO phase noise

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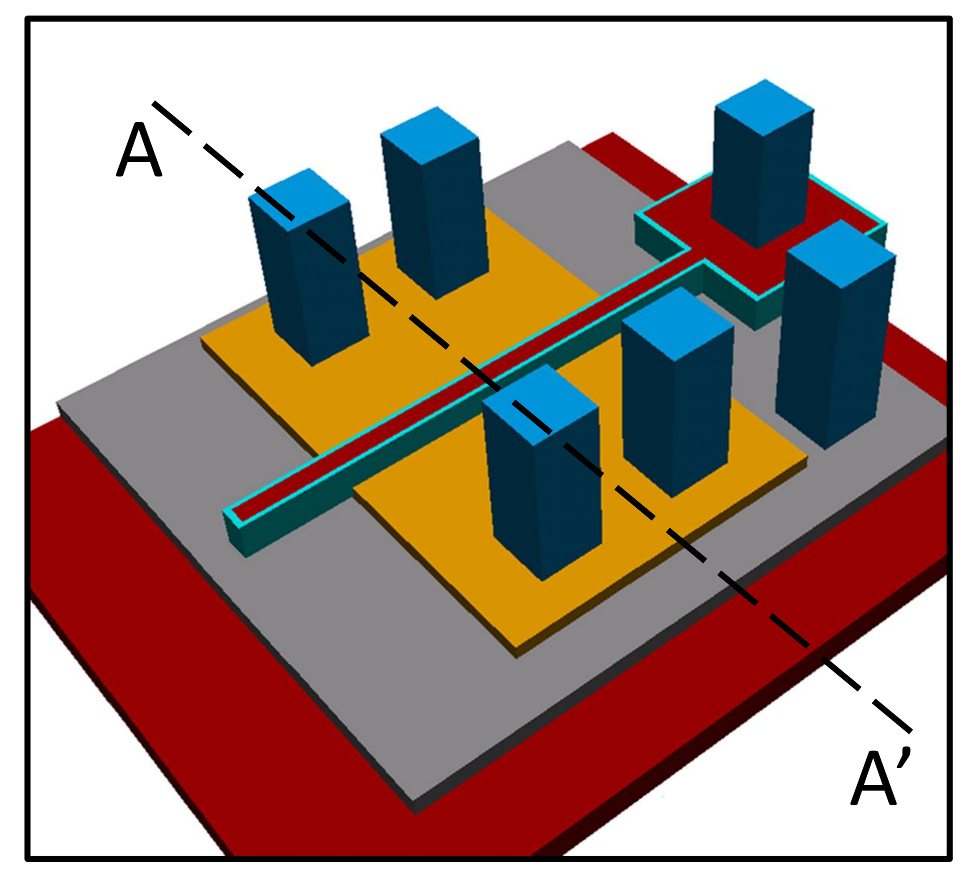
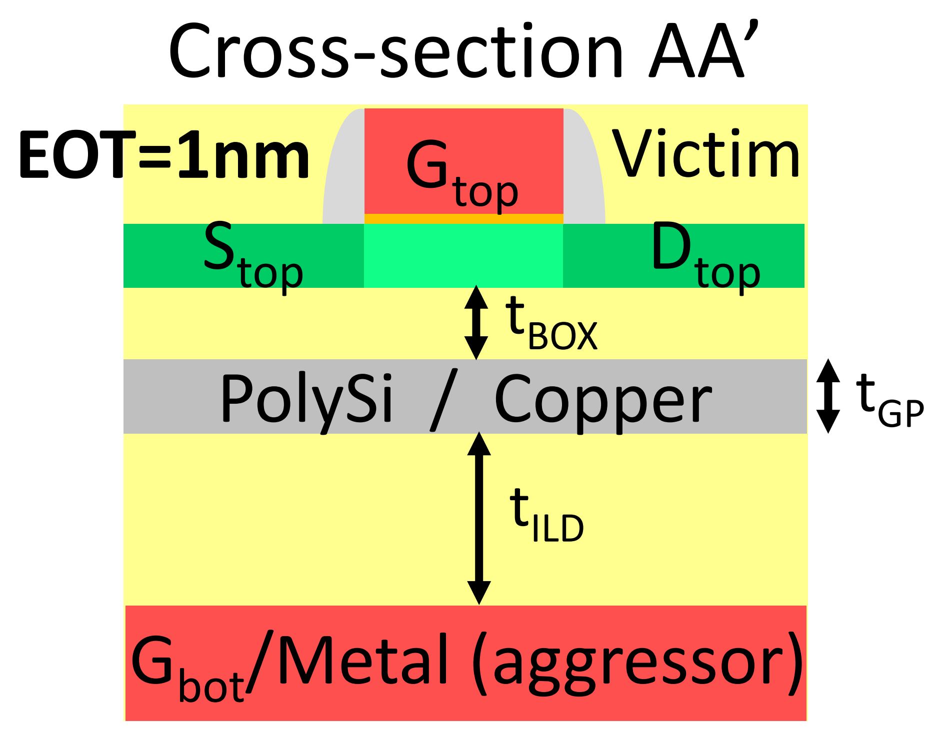
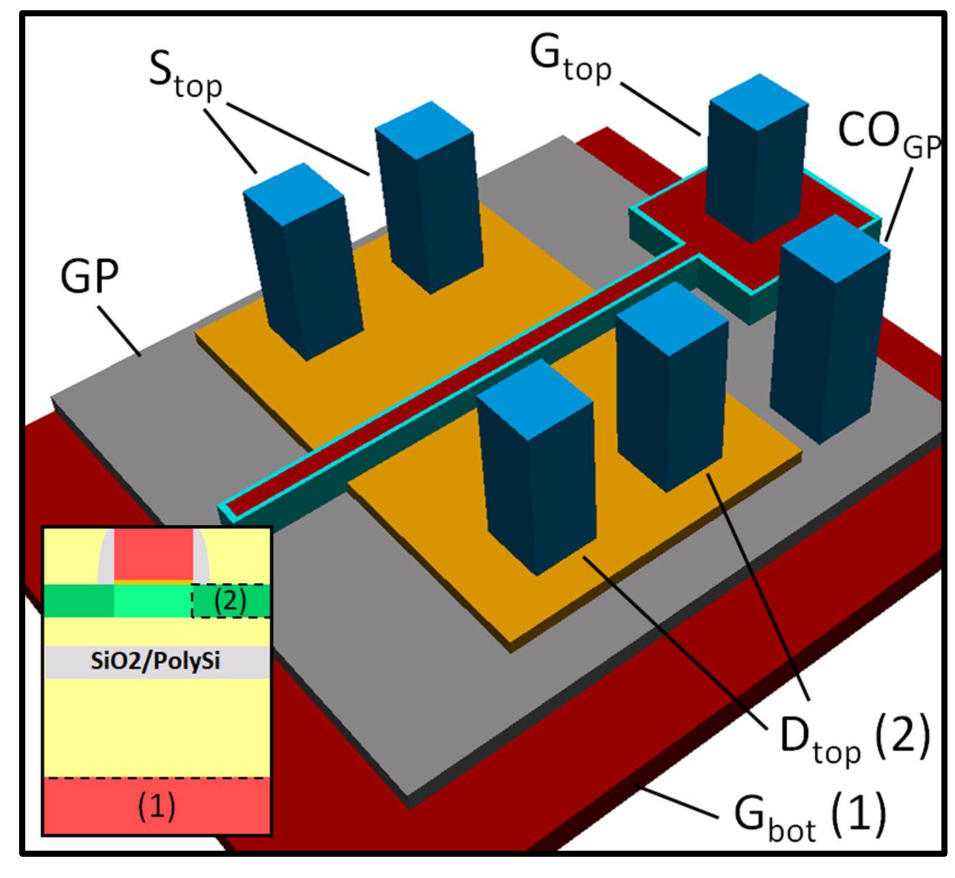
Ground Plane (GP) engineering

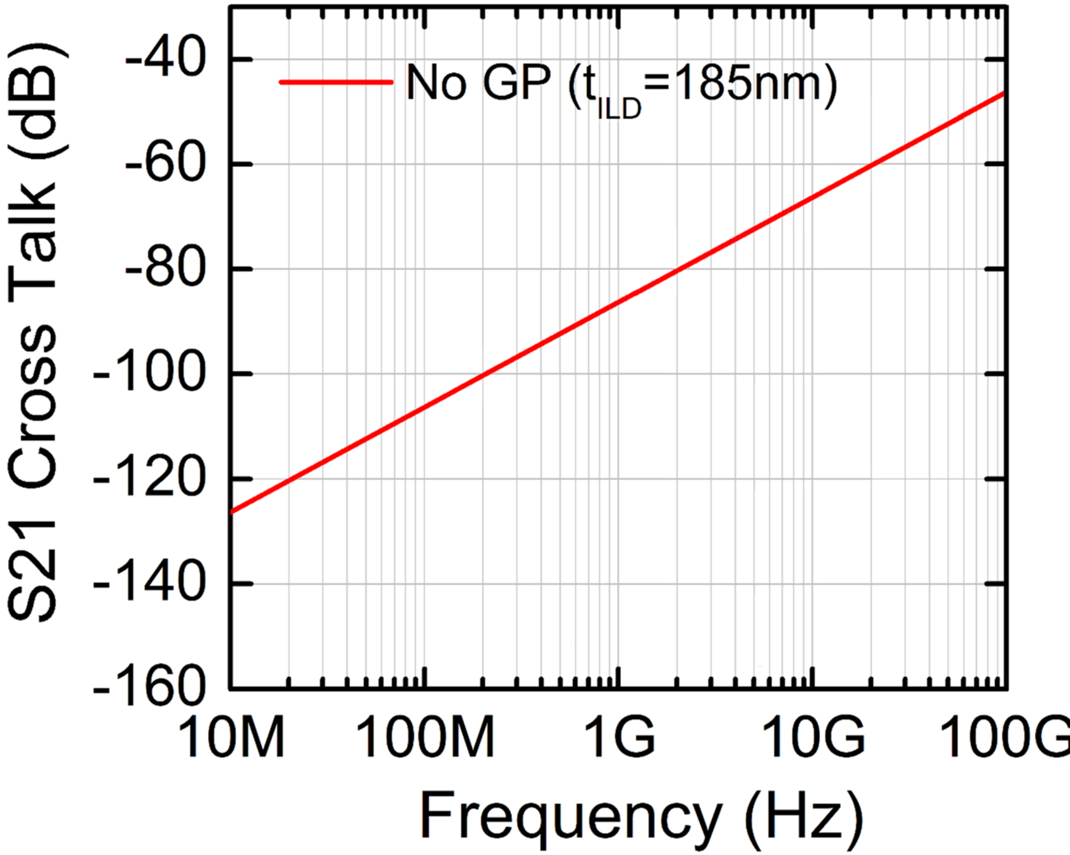




- Targets: Suppression level-freq., min. thickness, FEOL combatibility

GP RF crosstalk suppression





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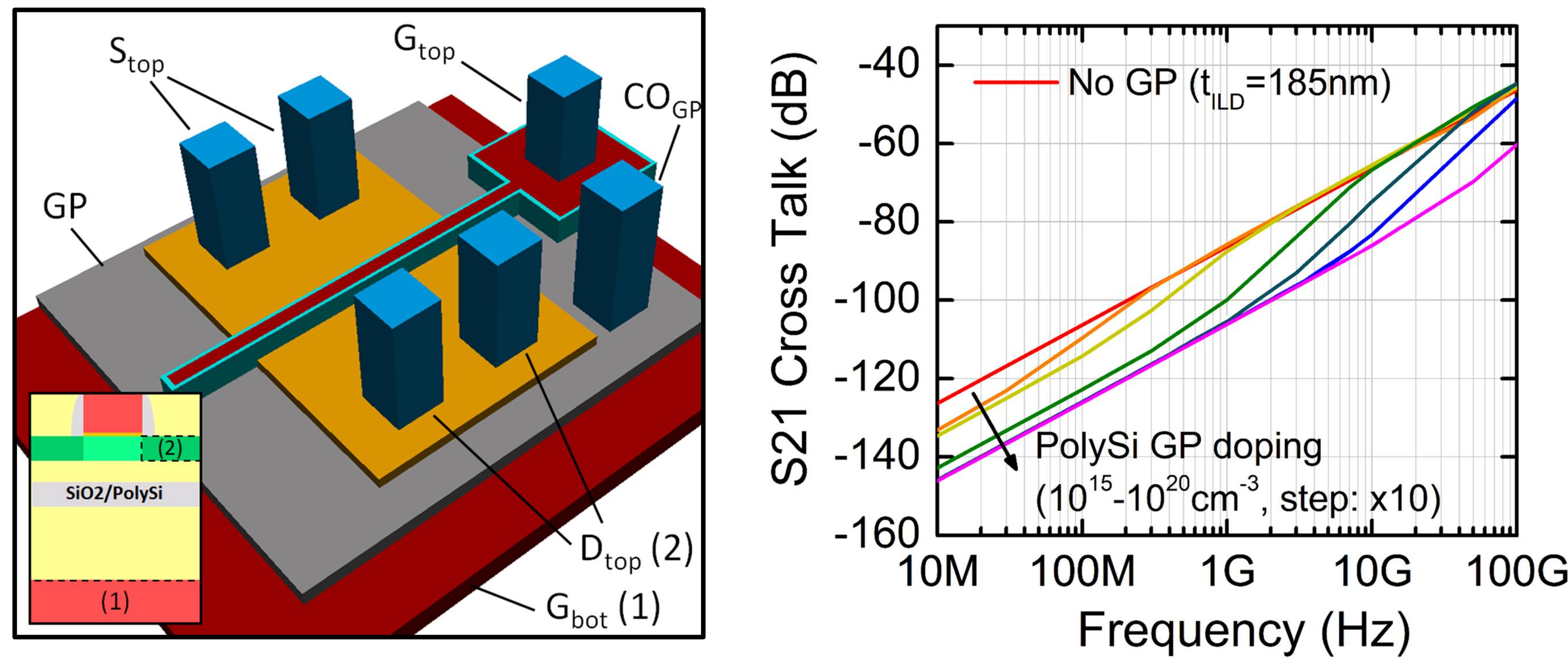
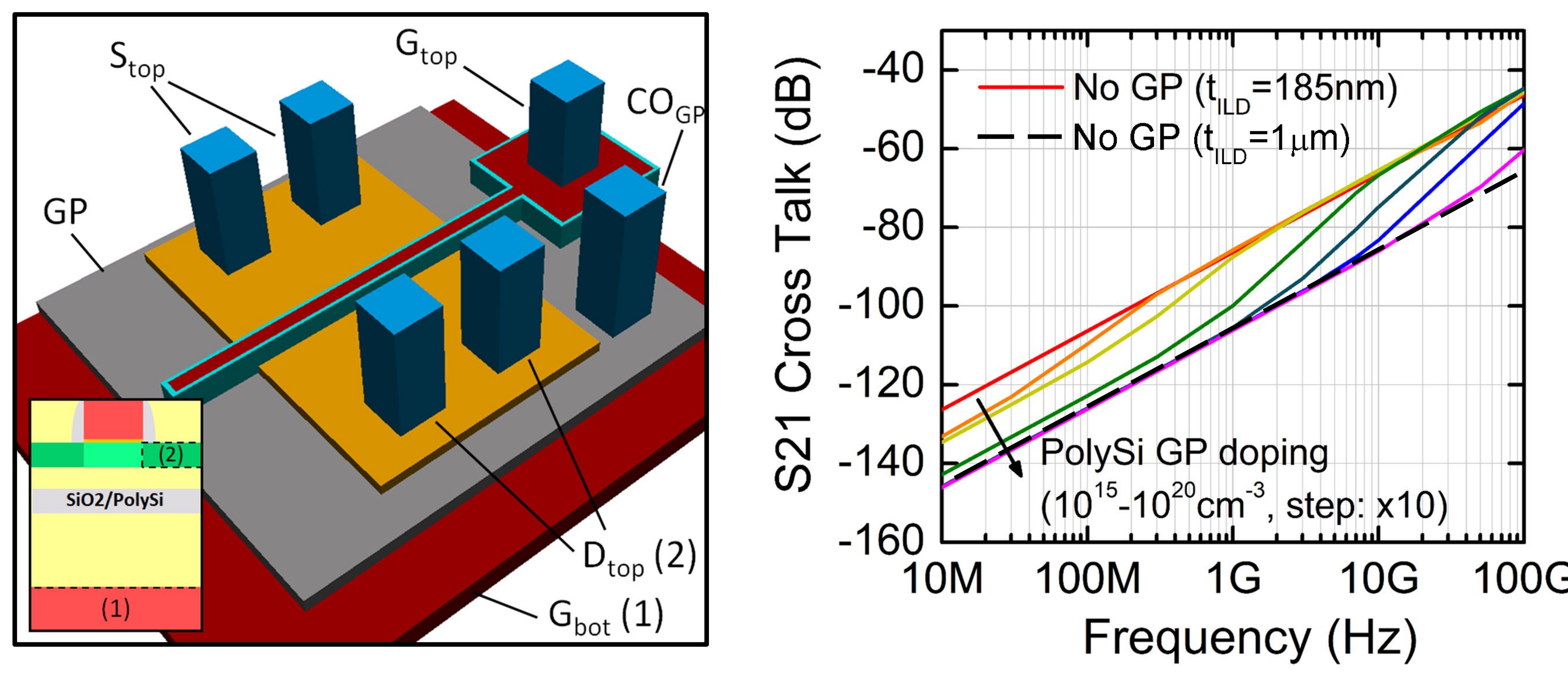


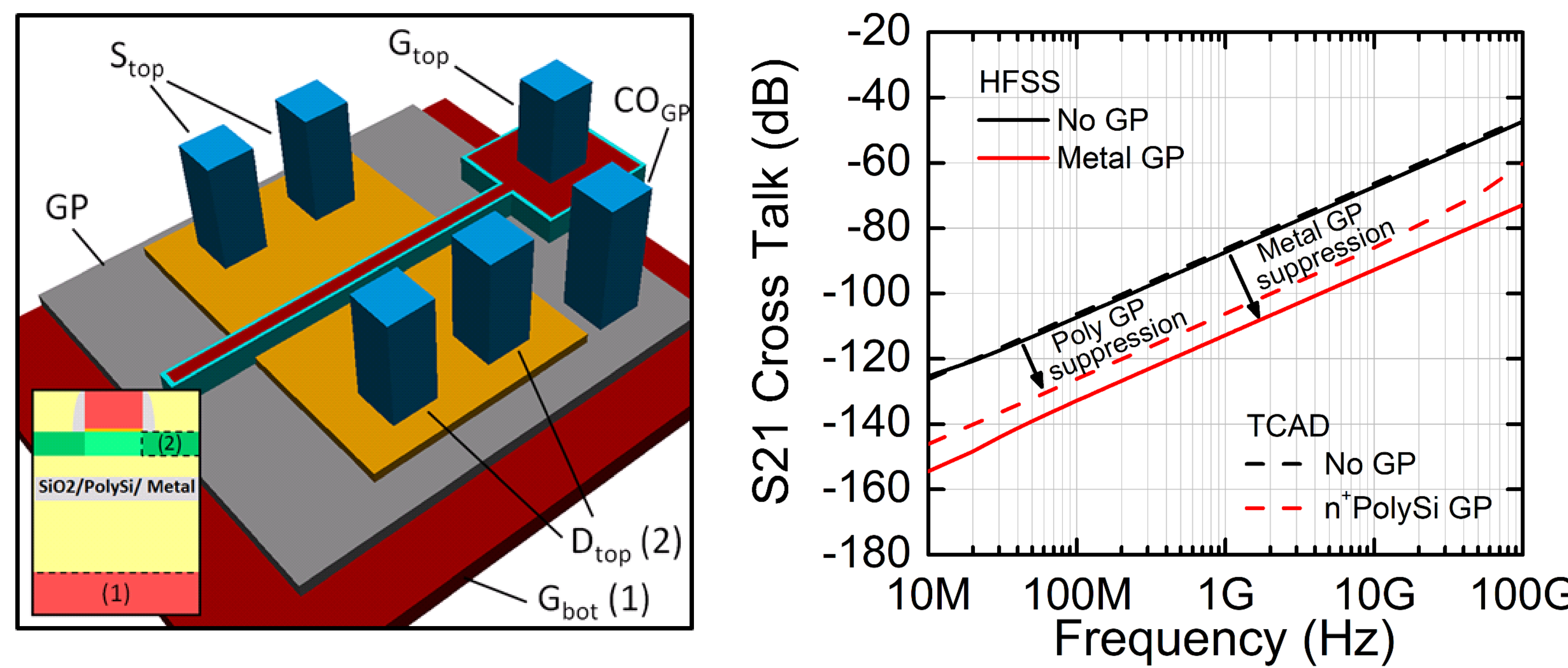
- n^+ polySi GP offers 20dB of suppression up to 100GHz

GP RF crosstalk suppression



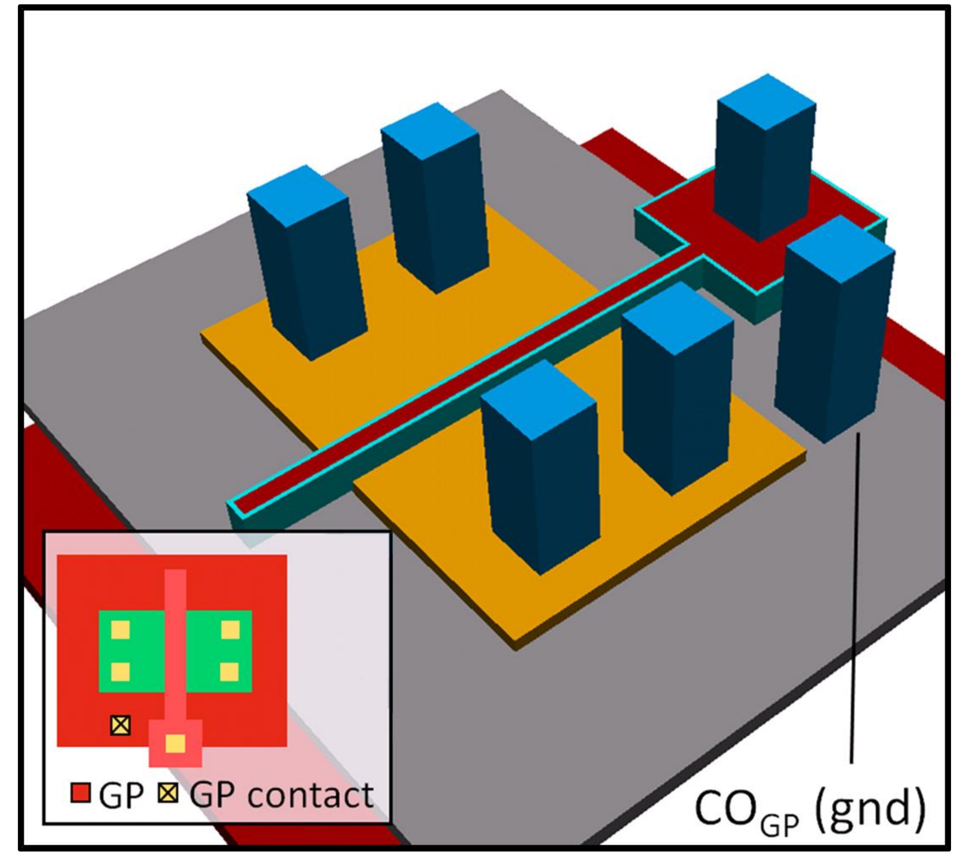
- n^+ polySi GP offers 20dB of suppression up to 100GHz
- GP insertion preserves 3D contact AR

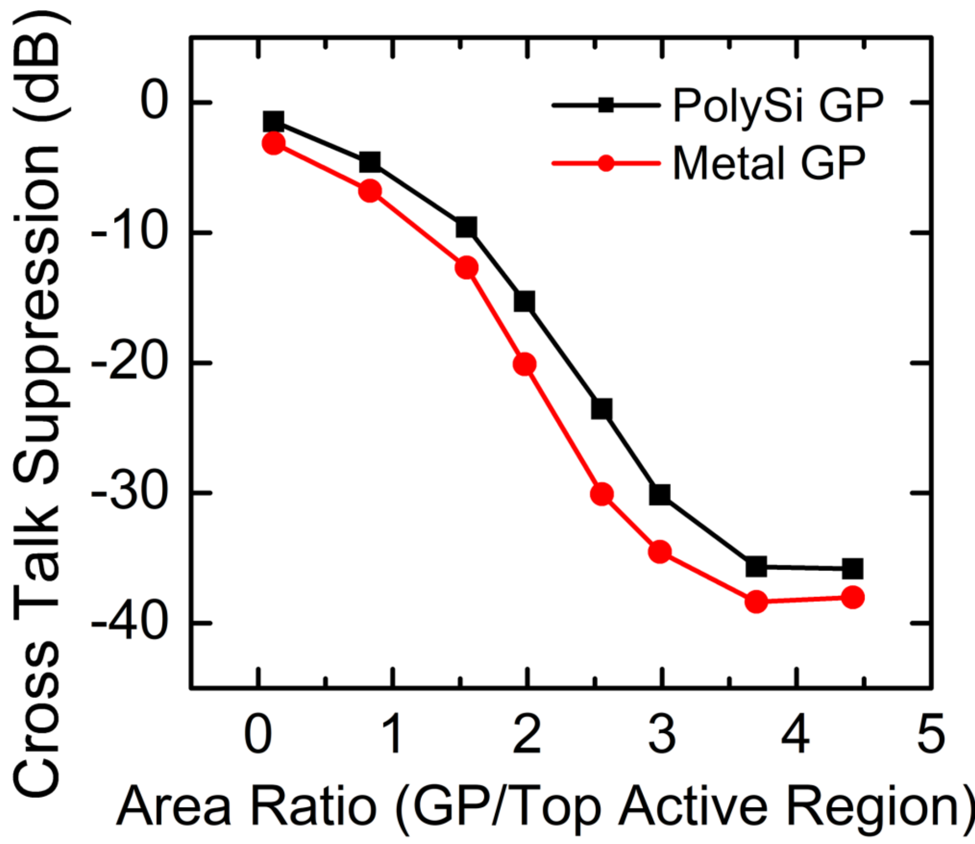
PolySi vs Copper GP



- n^+ polySi vs. Copper GP: comparable crosstalk attenuation

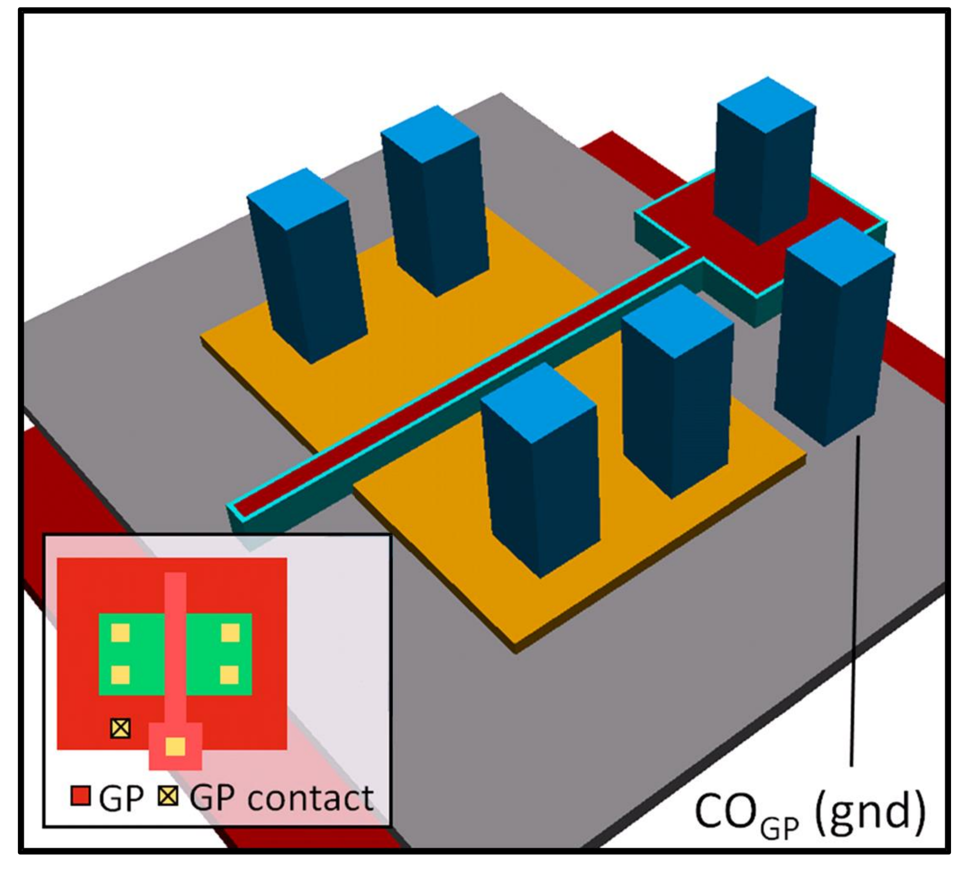
Impact of GP sizing

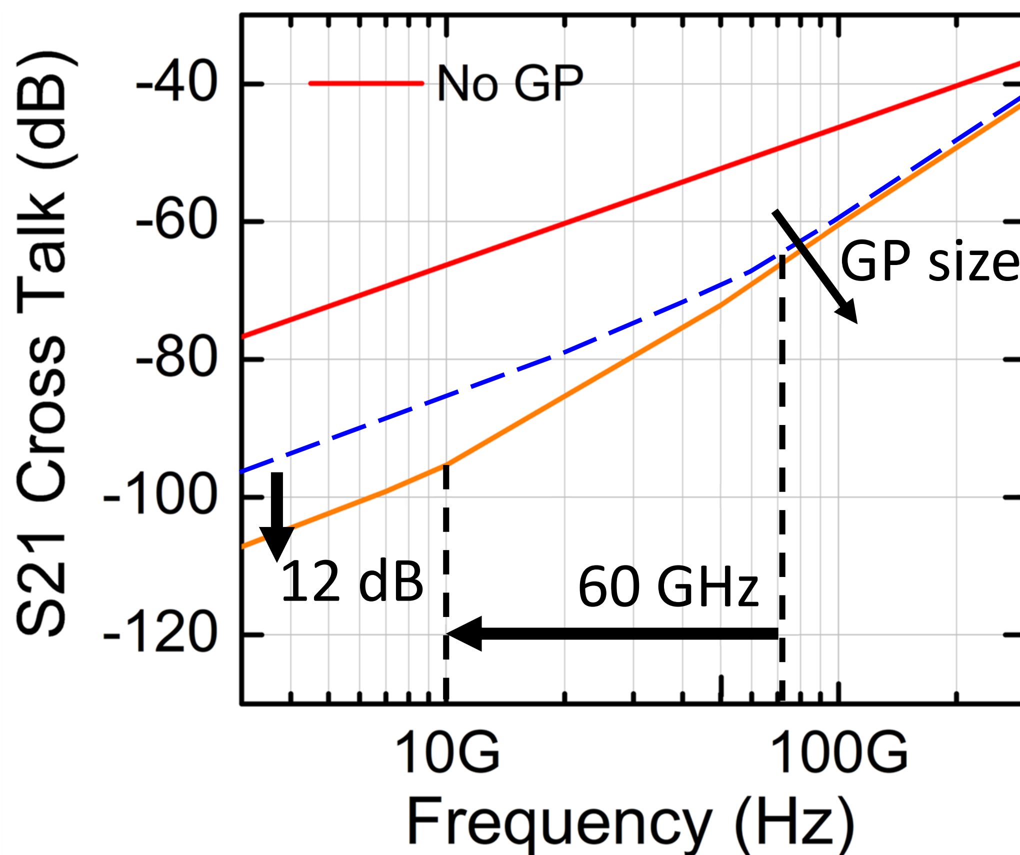




- Max. GP suppression → Max. covering of the top-tier SOI

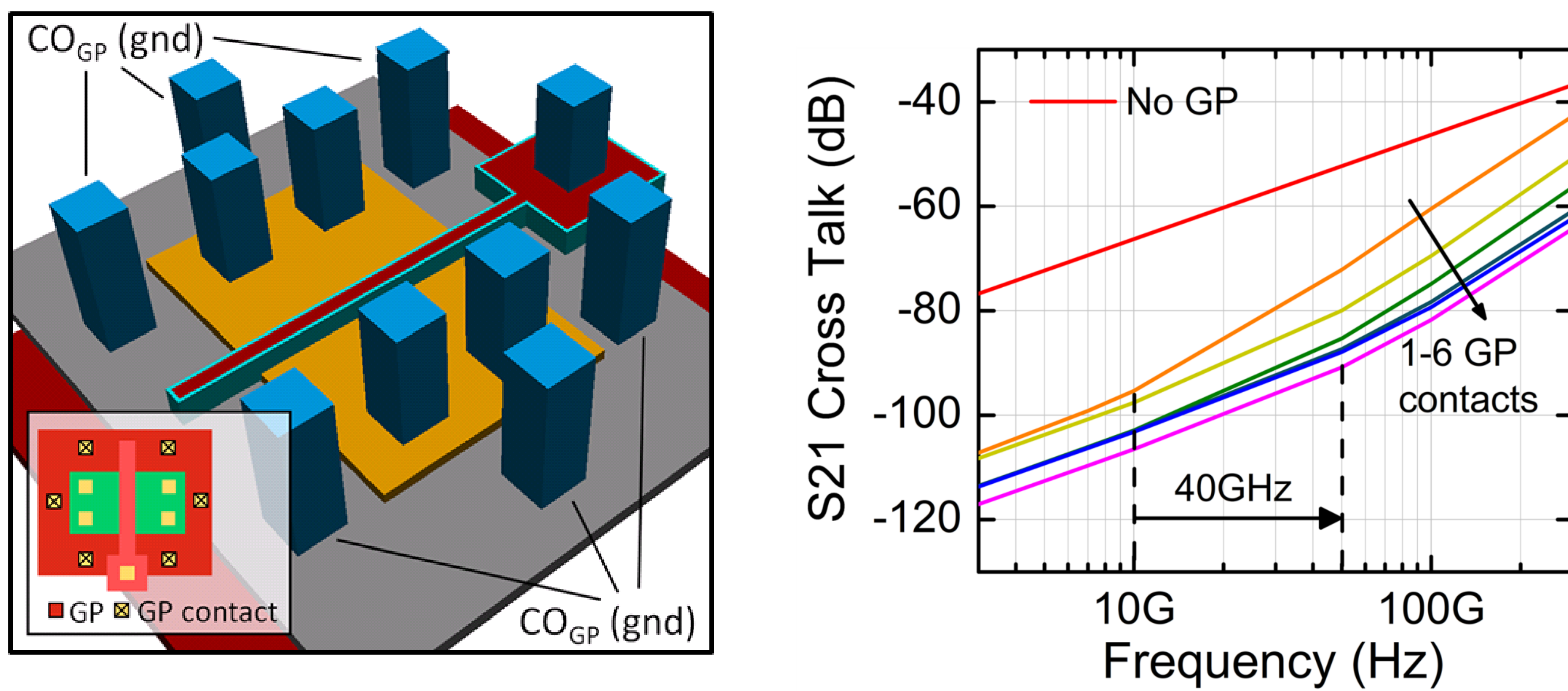
Impact of GP sizing





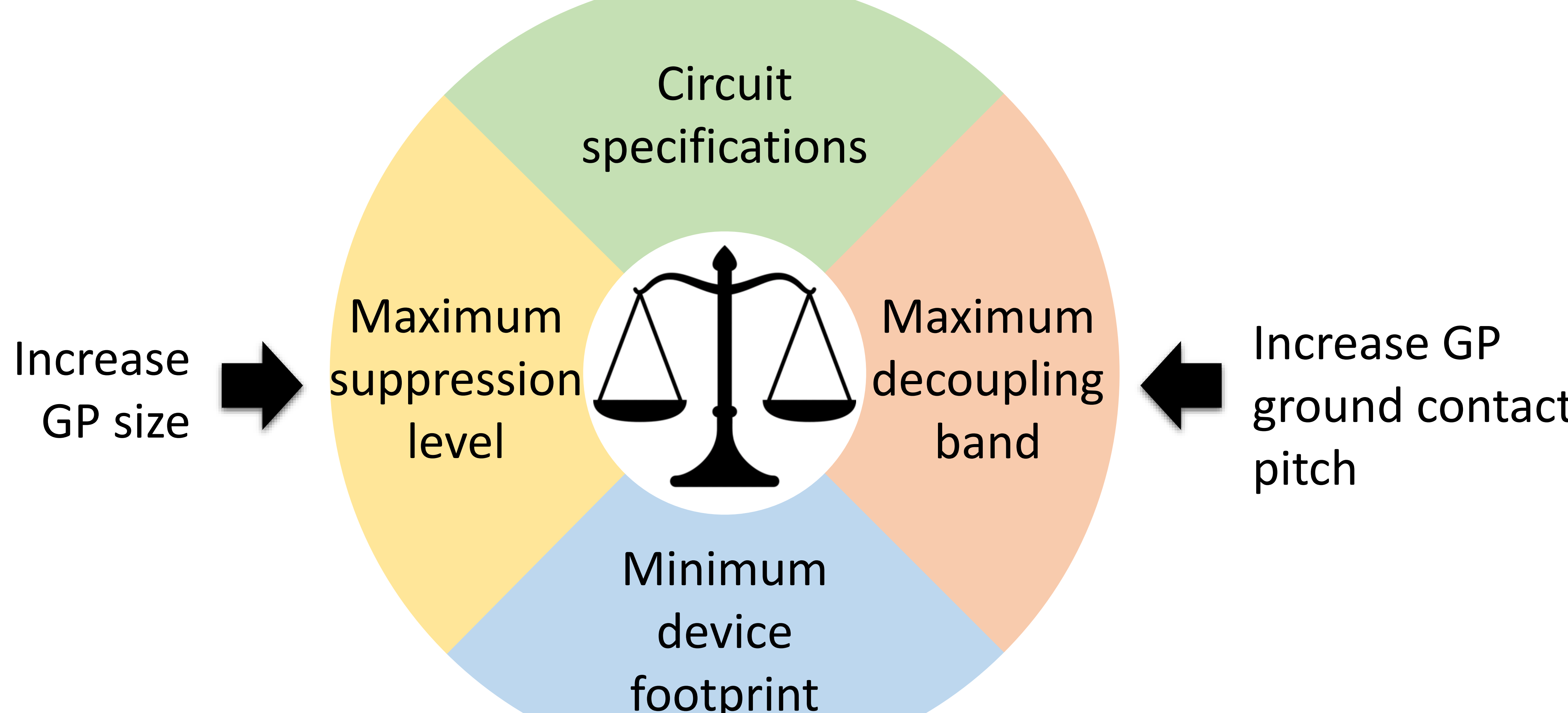
- Max. GP suppression → Max. covering of the top-tier SOI

Impact of GP ground contact pitch

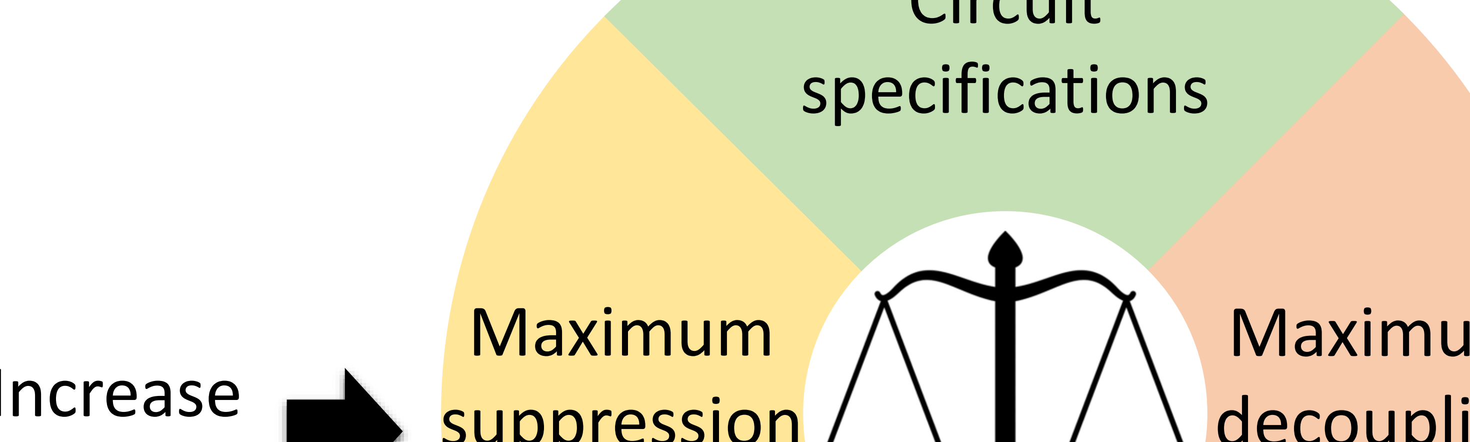


- Larger PolySi GP → more GND taps to retain the decoupling band

Optimum GP size & number of GND contacts



Optimum GP size & number of GND contacts



e.g. RF apps

- Max. GP covering
- Max. GND contacts

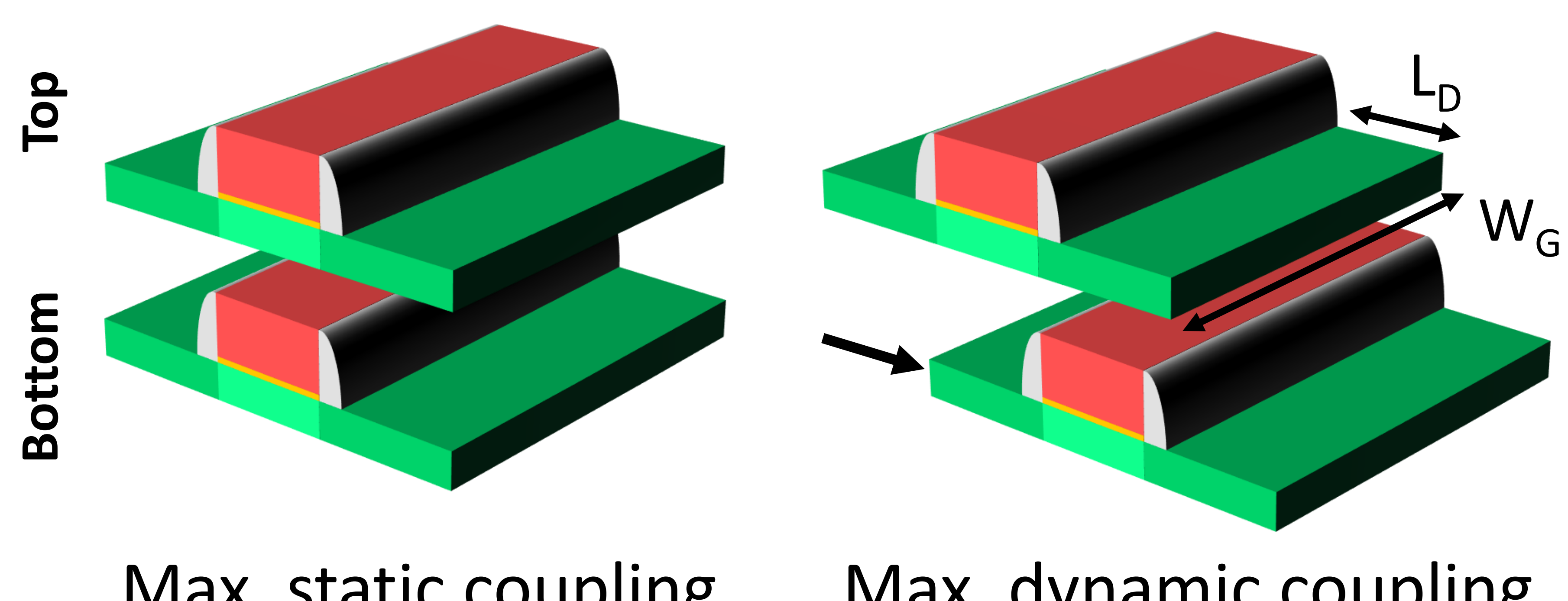
Increase GP ground contact pitch

Outline of Presentation

- Introduction/Motivation
- Device level results
  - Impact of static coupling
  - Impact of dynamic coupling
- Circuit level results
  - Impact of coupling on SRAM, RO
- GP morphology
- **Conclusions**

Summary

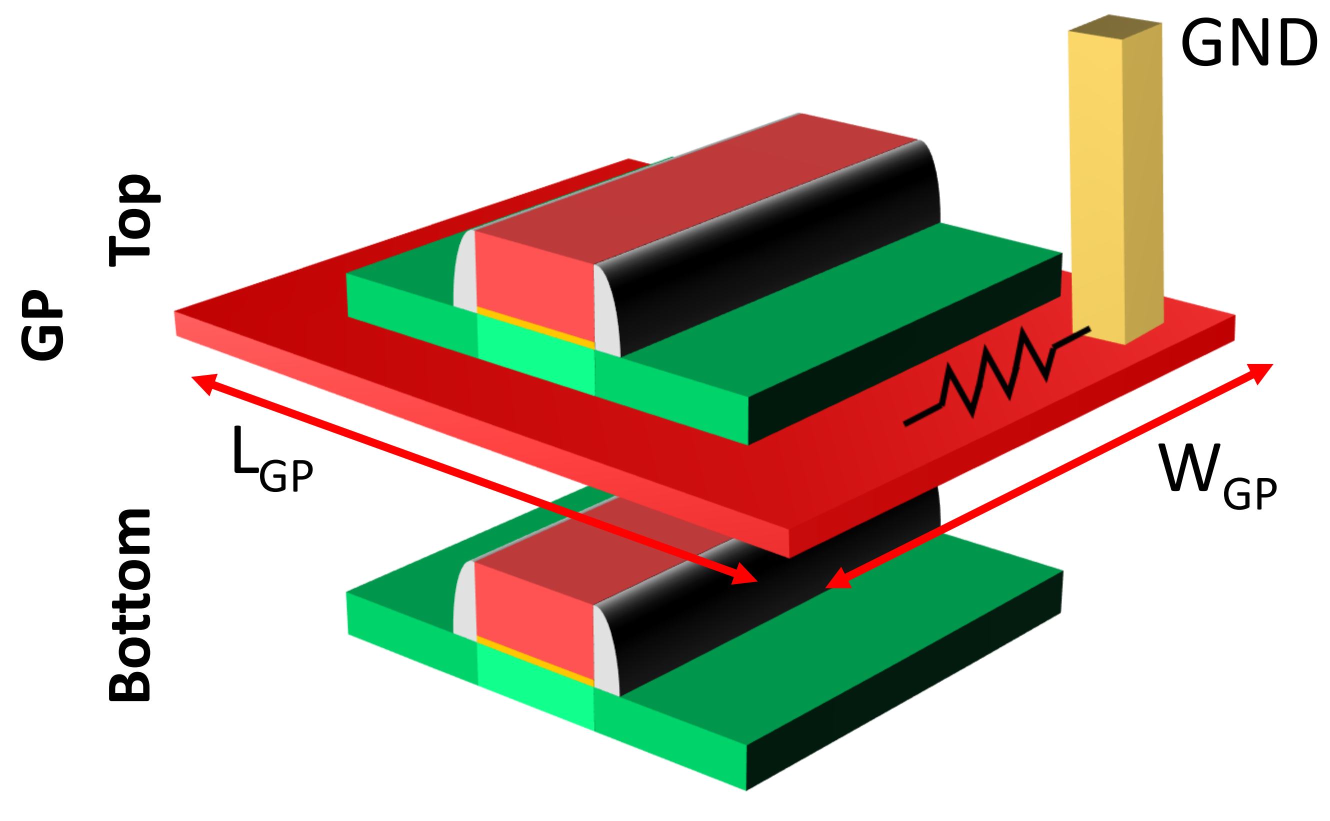
Intertier coupling effects



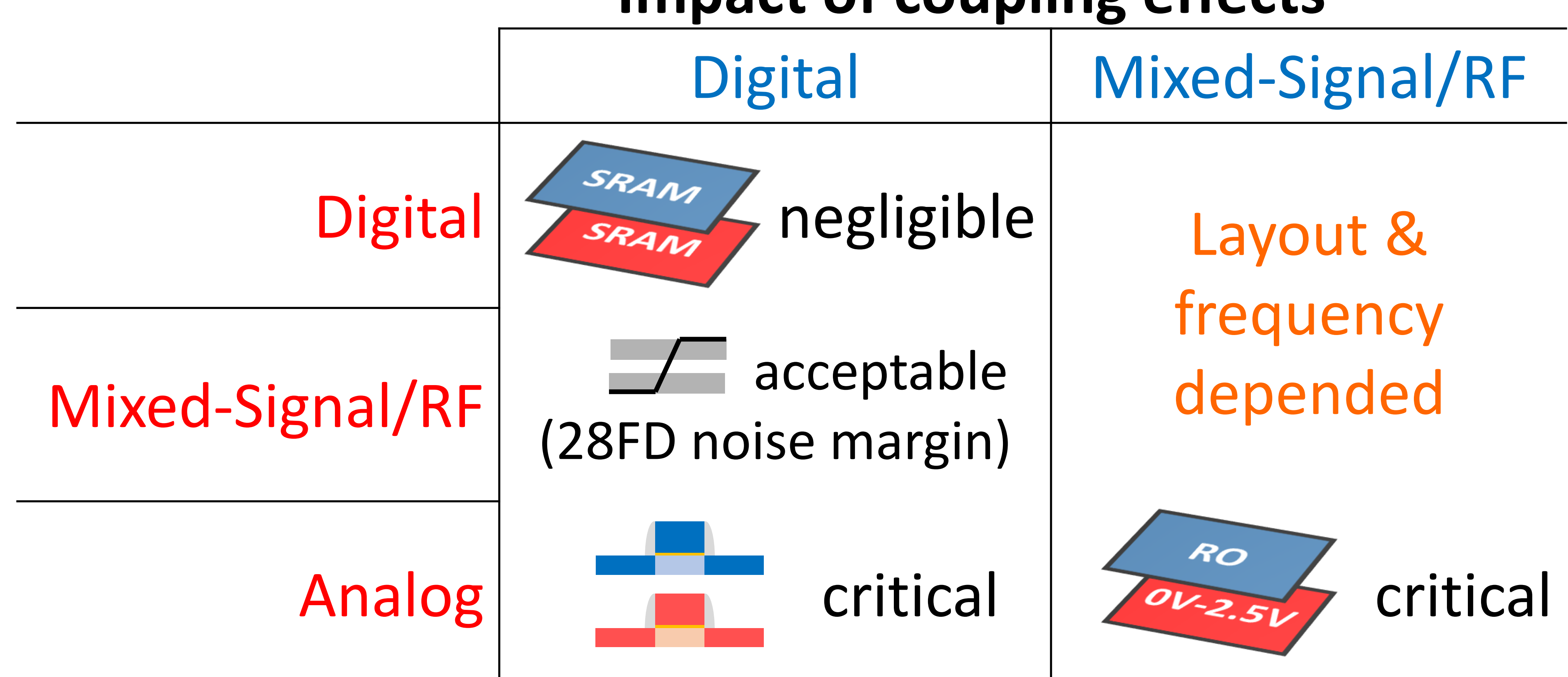
Max. static coupling

Max. dynamic coupling

Summary

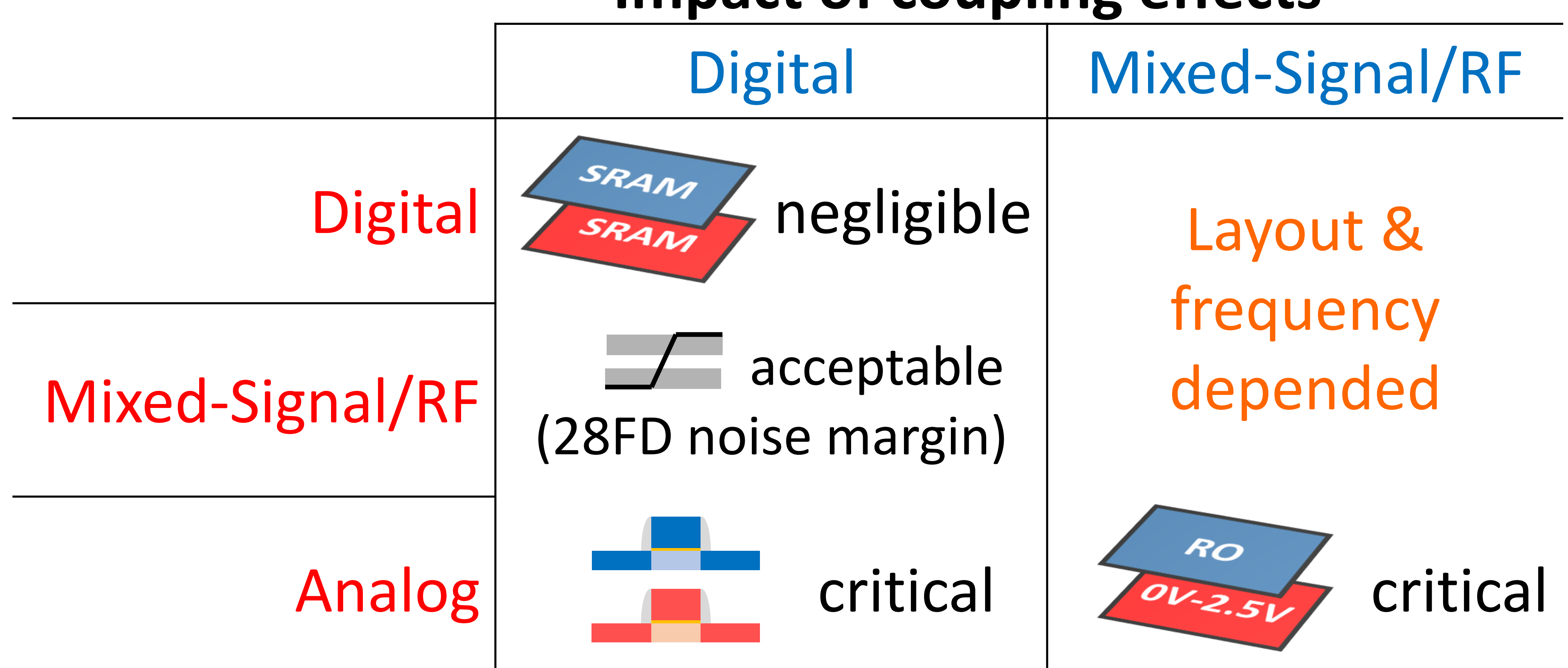


Summary


Impact of coupling effects

	Digital	Mixed-Signal/RF
Digital	negligible	Layout & frequency depended
Mixed-Signal/RF	acceptable (28FD noise margin)	
Analog	critical	critical

Summary



- GP → PolySi (FEOL), t_{GP}=34nm (3D contact AR), R_s = 295 Ω/□

Thank you for attending

More technical details:

- P.Sideris et al., EUROSOI 2019
- P.Sideris et al., SSE 2019
- P.Sideris et al., IEDM 2019

Questions?

Email: petros.sideris@cea.fr – Follow up questions related to this work

IMEP-LAHC, May 6, 2020

Coupling effects in Monolithic 3D technologies

A LabEX MINOS funded project | Starting year: 2017

Petros SIDERIS | PhD candidate

Gilles SICARD (leti/DACLE/SCCI/L3i) – Directeur de thèse
Perrine BATUDE (leti/DCOS/ LICL) – Co-Supervisor
Christoforos THEODOROU (IMEP-LAHC / CMNE) – Co-Supervisor